ME (Power Engineering) 1st Year First Semester 2025
Digital Systems

Time: 3hrs **Full Marks 100**

Answer all Questions

1. (i) **Represent** the states of a 3-bit synchronous **UP** counter as an FSM
   (ii) Using (i) **derive** the FSM for a 3-bit synchronous **DOWN** Counter
   (iii) **Derive** the circuit diagram of the UP counter using (i) **CO(1): 5+5+10**

2. Draw the schematic for a 555 timer based Astable Multi-vibrator and **deduce** the expressions for the Duty Cycle and Time period in terms of the Circuit Components used by you

   OR

   Imagine that a 555 IC is triggered at a frequency of 5KHz. Is it possible to produce a pulse train with Duty Cycle 0.4 using a capacitor and a resistor and this IC? If yes, **design** the circuit and suggest the component values or **establish** why it is not possible to realize the circuit.

   CO(2): 20

3. With the help of a neat schematic **explain** the functioning of a Totempole Circuit configured as a TTL NAND gate

   Or

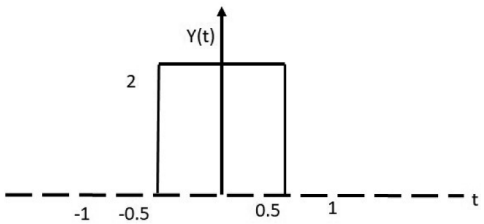
   With suitable assumptions, **derive** the (i) noise margin and (ii) fan-out for TTL family of logic circuits **Explain** the role of a pull-up and a pull-down resistor used in interfacing an open collector TTL gate with a CMOS gate. **Explain** which of the two logic families CMOS and TTL are faster and the reason behind it. **CO(3):20**

4. From first principles **derive** the Z transform of a signal $x(t) = e^{-at}, a > 0$ for a sample time of T_s. Is there a RoC for this-if so, derive the same. If this signal is delayed by N>0 samples, derive the corresponding Z transform.

   Or

   From first principles **prove** that $x[n] * h[n] = h[n] * x[n]$
   Express the following difference equation in the form of a branch diagram and hence deduce the Z transfer function $\frac{y(z)}{x(z)}$:
   $y[n] = a_1x[n] + a_2x[n-1] + a_3x[n-2] + a_5x[n-5]$ **CO(3):20**

5. **Derive** the Fourier Transform of the function shown in the Fig. below



   Or

   State and **prove** the Sampling Theorem from first Principles **CO(4): 20**