Ex/ET/PC/B/T/316/2025

B. ETCE THIRD YEAR FIRST SEMESTER EXAMINATION-2025

Subject: Analog CMOS Design and Technology Time: 3 Hours Full Marks: 100

All parts of the same question must be answered at one place only

Ensure neatness and clarity. Any approximation used in solving problems needs to be justified.

Use separate answer scripts for each part

PART-I (50 marks)
Model parameters for NMOS and PMOS device

Parameters	NMOS	PMOS
L_{min}	180nm	180nm
W_{min}	240nm	240nm
V_{th}	0.7V	-0.8V
λ (V^{-1})	0.1	0.2
μ (cm^2/Vs)	350	100
C_{ox} ($fF/\mu m^2$)	6	6

SECTION - A [CO1]

1. Answer **any Four** Questions: [Marks: 5×4=20]
   A) What is sub-threshold conduction? Why does MOS in sub-threshold produce a higher gain than MOS in saturation *(Explain with $log(I_D)$-V_{GS} plot)*?
   B) What is the channel length modulation effect? How the voltage-current characteristics are affected because of this effect?
   C) What is the trans-conductance (g_m) of a MOS transistor? Plot g_m-V_{GS} with V_{DS} as a parameter and g_m-V_{DS} with V_{GS} as a parameter.
   D) How does body bias change the threshold voltage of a MOSFET? Explain with a diagram.
   E) Explain why the circuits below cannot operate as a current source even though the transistors are in saturation.

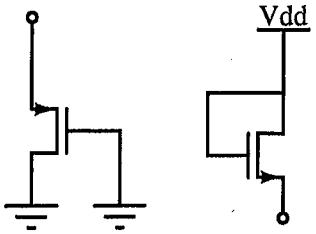


Figure 1

SECTION - B [CO2]

(Answer any Two)

2. Find the gain expressions of the amplifier circuits shown below. [Marks:15]
Consider $\lambda \neq 0$ and $\gamma \neq 0$.

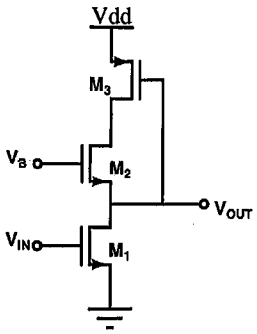


Figure 2

3. Find $\mathbf{I_X}$ vs $\mathbf{V_X}$ plot of the circuit shown below when V_X is varied from 0V to V_{DD}. Specify the voltage ranges corresponding to different transistor operating regions.
(Consider supply voltage V_{dd}= 3V, I_1=1μA(ideal), V_{THN}=0.7V and K = $\mu C_{ox}W/L$= 200 μA/V² and R_1 = 20KΩ) [Marks: 10+5 =15]

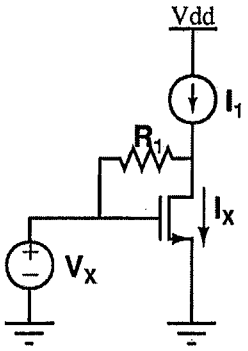


Figure 3

4. **A)** The circuit shown Below has following characteristics: V_B=2V, I_1=1μA(ideal), V_{THN}=0.7V and K = $\mu C_{ox}W/L$= 200 μA/V² with V_{BODY} =0V. If the initial voltage on the capacitor is 3V, **plot** V_X with respect to time. *(keep in mind that body to source conduction starts if $V_{SB} \leq$ -0.7V because of forward bias between body to source junction)* [Marks: 10]

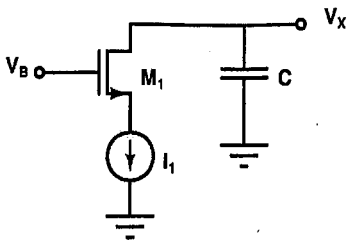


Figure 4

B) Find the Voltage V_X plot of the circuit with respect to time. *(Consider zero charge on the capacitor at time t=0).* [Marks: 5]

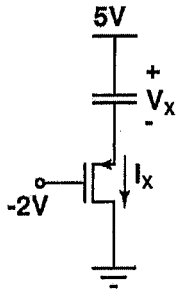


Figure 5

5. Design one CS Amplifier as shown below for voltage gain 20. [Marks: 15]

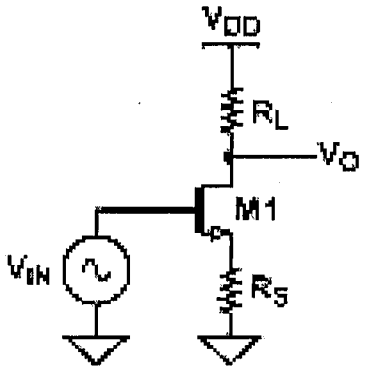


Figure 6

Ex/ET/PC/B/T/316/2025

BACHELOR OF ELECTRONICS AND TELE-COMMUNICATION ENGINEERING
THIRD YEAR FIRST SEMESTER EXAMINATION, 2025

Analog CMOS Design and Technology

TIME: **3 HOURS** FULL MARKS: **100**

Use separate answer script for each part

PART-II (50 marks)

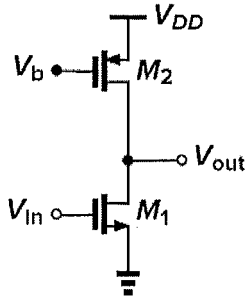
All parts of the same question must be answered together. The variable x in any of the following questions is equal to the last digit of your exam roll number.

Ensure neatness and clarity. Any approximation used in solving problems need to be justified.

SEGMENT – I (*Answer any ONE question*) **[CO-2]**

Q1.a) Discuss on the origin of *thermal noise* and *flicker noise* in an analog circuit. What is the *corner frequency* in this respect? 6

b) Considering both thermal and flicker noise, derive the expression of the output voltage noise spectrum for the following common-source amplifier. Hence find the rms noise voltage referred to the input terminal V_{in}. 12

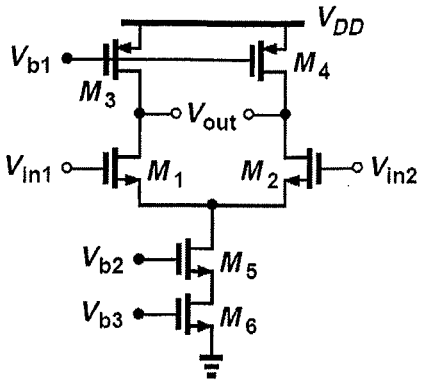


c) In the above circuit, if the width and length are both made $(x+2)$ times the initial values (for all transistors, keeping aspect ratio unchanged), explain how the corner frequency might change. 2

Q2.a) Draw the circuit diagram of a 5-transistor OTA and indicate which transistors of the OTA need to be matched. Discuss why such matching is necessary. 4

b) For low frequency operation of the following differential amplifier: (i) Derive the expression of the differential voltage gain, (ii) Draw its CM half circuit and hence derive the expression of its CM gain, (iii) Now assuming that $r_{o4} = (r_{o3} + \Delta r_o)$, derive the expression of its CM-to-DM gain ($A_{vCM\text{-}DM}$). What is the 14

expression of the CMRR of this circuit?



c) Discuss how the biasing of M_5 and M_6 can be achieved using a current mirror. 2

SEGMENT – II (*Answer <u>any ONE</u> question*) **[CO-3]**

Q3.a) Discuss how scaling of depletion widths is achieved during MOSFET scaling. 2

b) Draw the common-centroid layout of a 1:4 current mirror. Neatly indicate the different layers used and the circuit terminals in this layout. 6

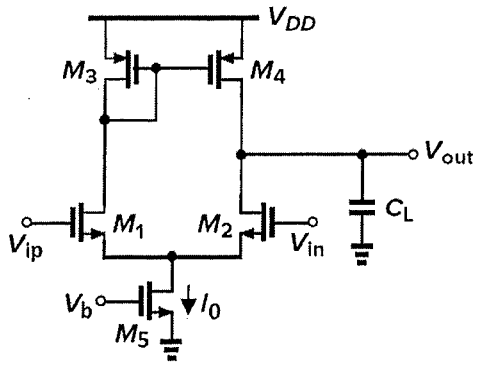
c) Describe the process of coating silicon wafer with photoresist. 2

Q4.a) "Velocity saturation can occur in both long and short channel MOSFETs" – discuss if this statement is correct with appropriate reasoning. 4

b) Illustrate the various steps in realizing self-aligned gate in CMOS process flow. 6

SEGMENT – III (*Answer <u>any ONE</u> question*) **[CO-4]**

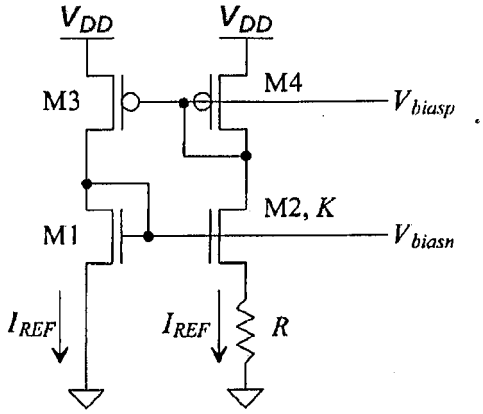
Q5.a) Design the width of the input-pair transistors to achieve: slew rate = (5+0.5*x) V/μs, UGF = 6*(5+0.5*x) Mrad/s, and dc power consumption ≤ 100 μW. Assume: C_L = 5 pF, V_{DD} = 2 V, $\mu_n C_{ox}$ = 200 μA/V^2, $\mu_p C_{ox}$ = 50 μA/V^2, λ_n = 80e-3 V^{-1}, λ_p = 30e-3 V^{-1}, and $|V_{TH}|$ = 0.5 V for all MOSFETs. Consider that the channel length L is (0.5+0.1*x) μm for all MOSFETs. 10



b) For the above circuit, will the power consumption and UGF increase or decrease due to an increase of the capacitive load C_L? 2

c) For the above circuit, design the width of the load transistors so as to achieve ICMR+ = 1.6 V and ICMR- = 0.9 V. 8

Q6.a) Derive the expression of current I_{REF} generated by the following circuit (neglect the finite output resistance of the MOSFETs). Note that the width of M2 is K times that of M1, while M3 and M4 have equal sizes. Hence, find the required value of the resistance R for generating a current of (1+0.3*x) μA. Use K = 4, V_{DD} = 1.8 V, $\mu_n C_{ox}$ = 300 μA/V^2, $\mu_p C_{ox}$ = 60 μA/V^2, $(W/L)_1 = (W/L)_3$ = 10. 10



b) Discuss (with appropriate circuit diagram) how the I_{REF} from the above circuit may be utilized to generate a current source of ($x \cdot I_{REF}$). 5

c) Draw the circuit schematic of a 5-transistor OTA where the above current source (as derived in part (b)) may be used to bias the OTA (try to utilize a minimum possible number of transistors in this circuit). 5