B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING
THIRD YEAR FIRST SEMESTER EXAM - 2025

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 hours **Full Marks: 100**

Answer questions from all five modules

MODULE 1 (Based on CO 1) **(20)**

1. a) Discuss any two metrics that can be used to measure the performance of a CPU. **2**
   b) State and explain the CPU performance equation. Briefly discuss, using this equation, how memory stalls can potentially affect the CPU performance. **3+2**
   c) Consider the following measurements:
   Frequency of floating-point (FP) operations (other than floating-point square-root (FPSQRT) operations) = 25%
   Average CPI of FP instructions = 4.0
   Average CPI of other instructions = 1.33
   Frequency of FPSQRT = 2%
   CPI of FPSQRT = 20
   Assume that the two design alternatives are to decrease the CPI of FPSQRT to 2 or to decrease the average CPI of all FP operations to 2.5. As a computer architect, which design will you prefer? Give quantitative validations. **10**
   d) Explain with a neat block diagram the Von Neumann architecture. **3**

MODULE 2 (Based on CO 2) **(20)**

2. a) Compare and contrast R-type and I-type instructions in MIPS. Give two examples from each of the above two instruction categories. **4+2**
   b) Consider the following MIPS code: **4**

```
LOOP: slt $t2, $0, $t1
      beq $t2, $0, DONE
      subi $t1, $t1, 1
      addi $s2, $s2, 5
      j LOOP
DONE;
```

   Assume that the registers $t1 and $s2 are respectively initialized to 10 and 0. What will be the contents of $t1 and $s2 after the execution of the above MIPS code? Explain your answer.
   c) Translate the above MIPS code into C. Assume that integer variables *i, B*, and *temp* exist in the registers $t1, $s2, and $t2 respectively. **6**
   d) Write the machine code for the instruction: addi $s2, $s2, 5. The opcode for the addi instruction is 8_{10}, and $s0 = 16_{10}$. **4**

OR

a) Explain the resources MIPS use to implement a procedure. **4**

b) Translate the following C function to MIPS procedure: **5**

```
void swap (int a, int b)
{
    int temp;
    temp = a;
    a = b;
    b = temp;
    return;
}
```

Assume $s1, $s2, and $t0 respectively hold the integers *a*, *b*, and *temp*.

c) Explain how MIPS uses a stack to implement recursive procedures. **3**

d) Translate the following recursive C function for obtaining the elements of the Lucas sequence to a recursive MIPS procedure: **8**

```
int Lucas (int n)
{
    if (n == 0)
        return 2;
    else if (n == 1)
        return 1;
    else
        return Lucas (n-1) + Lucas (n-2);
}
```

Clearly state the resources you are using for this implementation.

MODULE 3 (Based on CO 3) **(20)**

3. a) Show normalized scientific representation with 4 bits of precision, and IEEE 754 single precision binary representations of the two floating point numbers -0.5_{10} and 0.4375_{10}. **8**

   b) With a flowchart, show step-by-step calculation for obtaining the product of the two numbers in a). **7**

   c) Suggest how arithmetic instructions can adopt parallelism to support multimedia applications. Name any two relevant MPIS instructions in this context. **3+2**

MODULE 4 (Based on CO 4) **(20)**

4. a) Design a 32-bit MIPS ALU which can realize *AND*, *OR*, *add*, *sub*, *slt* and *NOR* operations. You should first show a 1-bit MIPS capable of realizing the above functions. **6**

   b) Differentiate between Ripple Carry Adder and Carry Lookahead Adder. How much faster would be a 16-bit Carry Lookahead Adder with respect to a 16-bit Ripple Carry Adder? **4**

   c) Explain how the following three different types of MIPS instructions are implemented – i) Arithmetic-Logical, ii) Load-Store, and iii) Branch **3+3+4**

MODULE 5 (Based on CO 5) **(20)**

5. a) What is cache memory? Why it is useful? **2+2**
   b) Define cache hit, cache miss, and miss penalty. **6**
   c) Suppose we have the following system: a processor with CPI 1.0 without any stall, a clock rate of 5 GHz, two levels of cache (primary, and secondary), miss rate of primary cache as 2%, miss rate to main memory as 0.5%, main memory access time as 200 ns and the secondary cache access time as 5 ns. As a computer architect, can you justify the inclusion of the secondary level cache for this system? Provide quantitative arguments. Further, analyze the performances (with and without secondary level cache) if the clock rate gets doubled. **10**

OR

   a) What is a direct mapped cache? Discuss using a diagram the design of a direct mapped cache with reference to cache index, tag field, byte offset and valid bit. **1+5**
   b) Discuss the relative merits and demerits of a direct mapped cache and a fully set-associative cache. **4**
   c) Consider the following sequence of block addresses: 0, 8, 4, 4, 4, 0, 6, 6, 8, 8. You are given a set of three small caches, namely, a direct-mapped cache, a 2-way set-associative cache, and a fully set-associative cache, each consisting of four one-word blocks. As a computer architect, design the best appropriate cache for the above sequence of block addresses. Provide quantitative validations. You may consider different block replacement policies in your design. **10**