Ref. No. Ex/ET/PC/B/T/413/2025

Department of Electronics and Telecommunication Engineering, Jadavpur University

B. E. Electronics and Telecommunication Engineering Fourth year 1st semester Examination 2025.

Attempt any five questions from Q1 to Q8 and all question carry equal marks. Q9 is compulsory.

Missing data may be assumed.

Subject : VLSI Design and Algorithm

Time : Three Hours Full marks : 100

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Q1. a). Why low power has become an important issue in the present day VLSI circuit realization?
b). Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics. What is noise margin? Find out the noise margin from the actual characteristics of the inverter.7+11 =18

Q2. a). What are different power dissipations in a CMOS circuits? Write the names of different parameters that control those power components. Explain how those parameters can be adjusted to reduce various power dissipation
b).Describe with necessary diagram, how will you reduce the propagation delay of an inverter? 14 + 4 = 18

Q3. Give the justification with proper explanation and diagram if any (related to Low power VLSI) for the following comments:
i). "Minimize activity on long bus"
ii). "Low Vth for speed critical circuits"
iii). "Lost performance can be compensated by parallelism"
iv). "Dynamic Power Consumption is Data Dependent"
v). "Use reduced supply voltage in sleep mode." 3+3+4+4+4 = 18

Q4. a). Why do we need memory in computers? Give detailed classification of memory along with brief about each of them.
b). What are Cache and Virtual memory? Explain Cache Miss, cache hit, Latency time and seek time.
c). Distinguish between Static and dynamic memory. Explain the working of compact Disc with neat diagram. 7+6+5 = 18

Q5 a). What is Cascode Voltage Switch Logic (CVSL)? Explain CSVL with an example.
b). Implement two-input (i) XOR and (ii) NOR gates with CSV logic. Explain their operations.
c). Explain CPL and DPL logic. 5+ 8 + 5 =18

Q6 a). For inverter design, why depletion load n-MOS inverter is preferred ? Explain the operation of TG – based NAND gate.
b). Design a two input XOR gate using CMOS logic. Explain fan-in and fan-out of logic gates.
c).How is a CMOS inverter different from a resistive load inverter? Which is preferred and why? 6+8+4=18

Q7. a). What are the limitations of CMOS inverter?
(b) Explain GDI logic with an example.
c). Implement two-input (i) XOR and (ii) NOR gates with GDI logic. Explain their operations.
d). Explain pseudo and Ganged CMOS logic. 2+3 + 8 + 5 =18

Q8. Write notes on any four of the following:
a) Body effect b) Parasitic Bipolar Effect. c). Mobility reduction by gate-induced surface fields d) Fringing field e) Constant Field Scaling versus Constant voltage Scaling f) Hot Carrier Effect 4x4.5=18

Q9. Choose the correct answer for each: 1x10 =10 ( question Q9 is compulsory)
(i). As die size shrinks, the complexity of making the number of die per wafer & photomasks
a) Increases , decreases, b) increases , increases , C ) decreases , decreases, d) decreases , Increases

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(ii) nMOS fabrication process is carried out in
a) thin wafer of multiple crystals , b) thin wafer of a single crystal
c) thick wafer of a single crystal , d) thick wafer of multiple crystals

(iii) As source drain voltage increases, channel depth
a) increases at the drain and source ends , b) decreases at the drain end
c) logarithmically increases at the drain end , d) exponentially increases at the drain and source ends.

(iv) Consider a p-channel MOSFET with $t_{ox}=600^0A$ and $N_D=5x10^{15}cm^{-3}$ . Find the body-to-source voltage , $V_{BS}$ , such that the shift in threshold voltage from the $V_{BS}=0$ curve is -1.5V .

a. 7.27V, b. 7.92V , c. 8. 24V , d. None

(v) The condition for non conducting mode is
a) Vds lesser than Vgs for Enhancement mode and depletion mode
b) Vgs = Vds = Vs = 0 for Enhancement mode only
c) Vgs lesser than Vds for Enhancement mode and depletion mode
d) Vgs = Vds = Vs = 0 for depletion mode

(vi) A BJT must dissipate 25watt of power. The maximum junction temperature is $200^0c$ , the ambient temperature is $25^0C$ , and the device to case thermal resistance is $3^0C/Watt$ . Find the maximum permissible thermal resistance between the case and ambient.

a. $5^0C/Watt$ , b. $4^0C/Watt$ , c. $4.5^0C/Watt$ , d. None

(vii) Consider a silicon PN photodiode at T = 300K with intrinsic layer width of 10 μm . If the incident photon flux is $10^{17}cm^{-2}\text{-}s^{-1}$ and the absorption coefficient is $3x10^3cm^{-1}$, calculate the prompt photocurrent density of the diode.

a. 14.85 mA , b. 15.2 mA , c. 15.62 mA , d. None

(viii) Find the temperature at which there is a $10^{-6}$ probability that an energy state 0.55eV above the Fermi energy level is occupied by an electron.

a. 423 K , b. 461K , c. 481K , d. None

(ix) Two scattering mechanisms exist in a semiconductor. If only the first mechanism were present, the mobility would be 250 $cm^2$ /V-s. If only the second mechanism were present, the mobility would be 500 $cm^2$ /V-s. Find the mobility when both scattering mechanisms exist at the same time.

a. 175 $cm^2$ /V-s , b. 167 $cm^2$ /V-s , c. 197 $cm^2$ /V-s, d. None

(x) ). Shot circuit power dissipation( in CMOS inverter) , Psc is eliminated
(a). If $V_{DD} \leq ( V_{THn} - |V_{THp}| )$ , (b). If $V_{DD} < V_{THn} + |V_{THp}|$ ,
(c). If $V_{DD} > (|V_{THp}| + V_{THn} )$ , (d). none of the a, b or c