BETCE 4th Year, 1st Semester Examination 2025

Subject: Electronic Design Automation (Elective paper)

Time : Three hours Full Marks : 100

Answer all questions from Q.1toQ.5. Each Question(Q.1 –Q.5)has two options Answer all the part of the question in same place. Different part of questions at different sections will carry no marks.

All the programme should follow proper syntax. Any kind of syntax error (semicolon , comma error, mismatch in identifier, wrong statement etc.) will carry no marks

Q.1 **A (CO-1)**

8+6+6=20

a. Write and explain briefly the steps of VLSI design cycle.
b. What are the difference between full custom and semi custom design?
c. Explain the significance of technology library and component library

Or

Q. 1 **B (CO-1)**

4+4+6+6=20

a. Briefly explain about Chiplet?
b. Explain the significance of PDK and its use.
b. What is logic synthesis and how it is carried out.
c. What is IP Core and write down their categories.

Q.2A **(CO-2)** **10+5+5=20**

a. Write a Verilog code of 8x1 using 4x1 and 2x1 MUX. Use primitive concept.
b. Write a Verilog code on Moore Machine.

Or

Q.2**B (CO-2)** **10x2=20**

a. Write a Verilog code of a two bit magnitude comparator using event based model. Write its test bench.
b.Design and implement a digital circuit that integrates a 3-to-8 decoder with a 3-bit priority encoder using Verilog.The 3-to-8 decoder should take a 3-bit input (A[2:0]) and produce 8 outputs (Y[7:0]), with an enable signal (EN) to activate the decoding.The priority encoder should encode the highest-priority active output of the decoder back into a 3-bit value (P[2:0]), where a higher index indicates higher priority.

Q. 3**A (CO-2)** **8+8+4= 20**

a. For a Sum of Product design what kind of timing hazard is possible? Explain with a case study. How to create a hazards free circuit?

b. What is the synthesized output of the following code?

```
module GrayToBinary (A, B, C, Bc0, Bc1, Bc2);
  input A, B, C;
  output Bc0, Bc1, Bc2;
  wire NotA, NotB, NotC;

  assign NotC = ~ C;
  assign NotB = ~ B;
  assign NotA = ~ A;

  assign Bc0 = (A & B & NotC) | (A & B & C) |
               (A & NotB & C) | (A & NotB & NotC);
  assign Bc1 = (NotA & B & C) | (NotA & B & NotC) |
               (A & NotB & C) | (A & NotB & NotC);
  assign Bc2 = (NotA & NotB & C) | (NotA & B & NotC) |
               (A & B & C) | (A & NotB & NotC);
endmodule
```

c. Discuss the impact of space complexity on the memory usage during synthesis, focusing on intermediate representations and lookup tables.

Or

Q.3B **(CO-2)** **6+8+6= 20**

a. Draw the synthesized circuit of following code. Use OAI logic as technology library

```
module SelectOneOf (A, B, Z);
  input [1:0] A, B;
  output [1:0] Z;
  reg [1:0] Z;

  always @ (A or B)
    if (A > B)
      Z = A;
    else
      Z = B;
endmodule
```

b. Explain with example about Gate Merging, Sub expression elimination and Power Optimization in synthesis.

c. Write down the flowchart on the steps to set up the synthesis environment in Synopsys Design Compiler, including setting up libraries, constraints, and design files.

Q. 4A **(CO-3)** **5+5+10=20**

a. How zero bias threshold voltage is modeled in SPICE level 1? Draw clear diagram of equivalent circuit of MOSFET for AC noise analysis

b. The MOSFET has an initial channel length L of 1 μm and operates at a supply voltage VDD of 5V. The oxide thickness tox is 10 nm. To maintain reliability and avoid breakdown due to high electric fields, constant field scaling is applied with a scaling factor S=1.5.Determine the following:

1. The new values of channel length L′, supply voltage VDD′, and oxide thickness tox′ after scaling.

2. The impact of scaling on current density and power density in the MOSFET.

Or

Q.4B **(CO-4)** **5+5+5+5= 20**

a. What are the designable and noise parameters? Explain with an example of inverter circuit.
b. Draw the PVT corner diagram. What are the front end line corner parameters in timing corner?

Q.5 A **(CO-4)**

4+6+10 = 20

a. Explain the bathtub curve for reliability.
b. Why response surface are used and how the global and local maxima of convergence are achieved from RSM contours.
c. A CMOS chip with three signal input terminals, one output terminal, one power supply terminal, and one ground terminal. The input signal voltages can vary from 0 to 5 V, the power supply voltage can vary from 4.5 V to 5.5 V, and the device operating temperature can range from 0 to 85 ^{0}C. We want to design an experiment so that the DC response of the chip can be described by a quadratic response surface model for three inputs, power supply voltage, and temperature.
Design a full factorial experiment.

Or

Q.5B **(CO-5)**

4+6+10 = 20

a. Brief explains ANOVA and justifies the usage of ANOVA in Surface model
b. Draw the flowchart to generate response surface model (RSM) in comparison to SPICE model. Write down the multi variable equation for RSM with inner products.
c. In the following circuit X_4 has a S-a-0. For a test vector 1001 that detects error find out fault