# Bachelor of Instrumentation and Electronics Engineering, 2025
## 2nd year, 1st semester
## DIGITAL ELECTRONICS

**Time : Three hours** **Full Marks : 100**

**ANSWER ALL MODULES**

### Module – I (4 Marks)

Q1. What decimal number corresponds to the binary pattern **10101100**, when it is in

(a) **Excess-3 BCD** format, (b) **1's complement** format, (c) **2's complement** format, and (d) **Gray** format. (4)

### Module – II (6 Marks)

Q2. Perform the following arithmetic operations :

(a) **(+52) + (+76)** using **8-bit 2's** complement number system.

(b) **(368) + (2093)** using Excess-3 BCD numbers.

**Represent the final results in decimal**. (3+3)

### Module – III (40 Marks)

**(Answer Q3 and ANY ONE from Q4 and Q5)**

Q3. (a) Why are **CMOS transmission gates preferred** over both **n-MOS and p-MOS pass transistors** for connecting signals to a bus ?

(b) Draw the circuit of a **2-input tristated TTL inverter** with totem-pole output.

(c) Draw the CMOS circuit to realize a **Full-adder**. (5 + 5 + 10)

Q4. (a) Use **Karnaugh Map** technique to obtain the minimized expressions for the following functions as indicated :

(i) **F(W, X, Y, Z) = W'Y'Z' + WX'Y' + XY'Z + W'X'Y' + WX'Z + W'XZ' + WXYZ'**; using **only NOR** gates

(ii) **F(A, B, C, D) = $\prod$M (3, 6, 9, 11, 12, 14) + d(0, 1, 4, 10)**; in **minimized SOP** form

(iii) **F(A, B, C, D) = $\sum$m(0, 1, 2, 6, 8, 10, 11, 12)**; in **minimized POS** form

(b) Realize a **Full-adder** using a suitable **PROM** of **minimal configuration**. **Draw** the **necessary diagram**. (3 x 5 + 5)

Q5. (a) With the help of an example, explain how the occurrence of overflow in 2's complement arithmetic is detected. Using **one 4:1 Multiplexer** and **one 2:1 Multiplexer (if needed)** realize the logic circuit for this overflow detection. **Draw** the **necessary diagram**. (3 + 7)

(b) Using a suitable decoder and necessary logic gate(s) realize the following functions :

**f1 = WX'Y' + XY'Z + W'X'Y' + WX'Z + W'XZ'**

**f2 (W, X, Y, Z) = ΠM(0, 3, 4, 7, 9, 11, 13, 14)**

**Draw** the **necessary diagram**. (10)

## Module – IV (50 Marks)
## (Answer Q6 and and ANY ONE from Q7 and Q8)

Q6. (a) Design a **sequence detector** which **detects the input sequence "101" including overlapping.** The output will be Logic 1 whenever this sequence is detected. Otherwise, the output will remain Logic 0. **Use D-FFs** as the memory elements. (15)

(b) Realize a **T-FF using SR-FF** as the memory element. (10)

(c) Draw the circuit diagram for a 4-bit Serial Input Parallel Output right shift register using D-FFs as memory elements. Where might this register be used ? (4 + 1)

Q7. (a) Design a **Lock-out free** synchronous **binary Mod-6 counter**. Use **T-FFs** as memory elements. (14)

(b) What is the **Race-around problem in JK Latch** ? **Explain**. (6)

Q8. (a) Design a sequence generator which generates the sequence "**1101000**" repeatedly. Use minimum number of **D-FFs**.

(b) Using **JK-FF** as memory element, realize a sequential **Gray to Binary** code converter. The input Gray bits are **coming serially starting from the MSB**. (10 + 10)

-------- * --------