Ref. No.: Ex/IEE/PC/B/T/214/2025

B. INS. & ELEC. ENGINEERING 2ND YEAR 1ST SEMESTER EXAMINATION 2025

ELECTRONIC CIRCUITS

TIME: 3 HOURS **FULL MARKS: 100**

List of Course Outcomes (CO):

CO1: Classify and analyze different types of diode circuits (K2, K4, A1)

CO2: Identify and interpret the importance of biasing in electronic amplifiers (K3, A1)

CO3: Describe and explain the behavior of small signal amplifiers (K2, A1)

CO4: Differentiate and examine feedback circuits of various kinds (K4, A2)

CO5: Explain and analyze the operation of oscillators (K2, K4, A1)

Instructions to the Examinees:

- Each module in the question paper matches up with the corresponding CO
- Attempt **ALL** the questions from **ALL** the modules for the attainment of all the Cos
- Alternative questions (if any) exist within a module, not across the modules

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Ref. No.: Ex/IEE/PC/B/T/214/2025

MODULE 1

ATTEMPT **ANY TWO** QUESTIONS FROM THIS MODULE

1. Show the voltage waveform across each half of the secondary winding and across the load resistor when a 100 V peak sine wave is applied to the primary winding in Fig. 1. What minimum PIV rating must the diodes have?

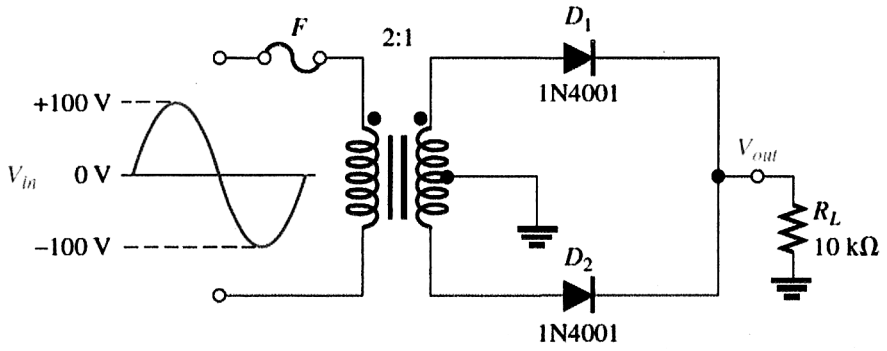

Fig. 1

6+4

2.

(a) Draw and explain the operation of a positive clipper circuit. Draw the transfer characteristics of such a circuit when constructed using practical diode with a cut-in voltage of 0.65 V.

(b) Show the effect of capacitor in eliminating the ripple content from a rectified output voltage.

(3+2)+5

3. For the circuit in Fig. 2, determine the output voltage at minimum and maximum zener current. Calculate the value of R that should be used. What is the minimum value of R_L that can be used? Given $V_Z = 15\ V\ @\ I_Z = 17\ mA, I_{ZK} = 0.25\ mA, Z_Z = 14\ \Omega$ and $P_{max} = 1\ W$.

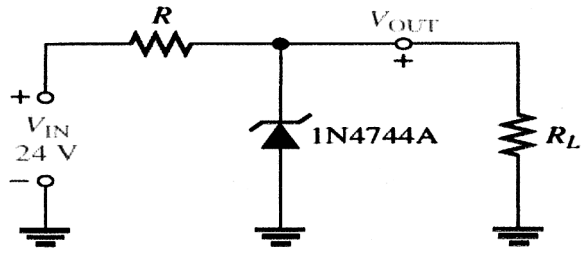

Fig. 2

5+5

Ref. No.: Ex/IEE/PC/B/T/214/2025

MODULE 2

ATTEMPT **ANY TWO** PARTS FROM **Q. NO. 4**

4.

(a) Find out the expression for quiescent collector current for a collector-feedback bias circuit.

(b) Determine whether or not the transistor shown in Fig. 3 is in saturation. Assume $V_{CE(sat)} = 0.1\,V$.

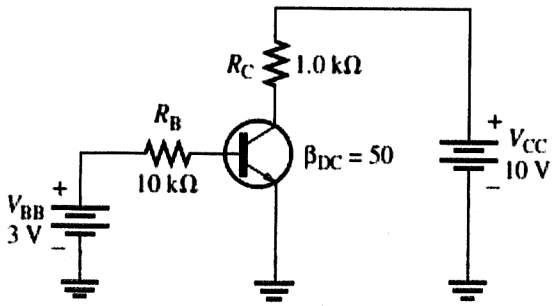

Fig. 3

(c) What is the significance of load line? How can the slope of the load line be adjusted?

(d) Mention the basic difference between stiff and non-stiff voltage divider bias.

2X5

MODULE 3

ATTEMPT **Q. NO. 5 AND ANY ONE** FROM THE REST

5. For the common emitter amplifier shown in Fig. 4, calculate (i) the mid-band gain (ii) 3-dB bandwidth using appropriate graph paper. The transistor's datasheet provides the following: $\beta_{dc} = \beta_{ac} = 80, V_A = \infty, c_\pi = 20\,pF, c_\mu = 2.4\,pF$. Consider appropriate number of frequency points both in the low and high frequency range in drawing the frequency response. Assume $V_T = 25\,mV$.

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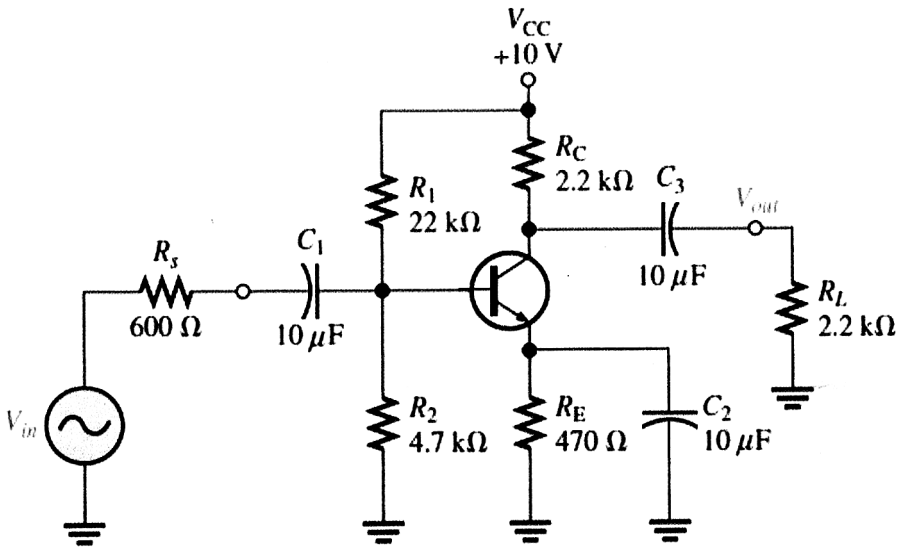

Fig. 4

10+30

6. Show that the small-signal voltage gain of a common-base amplifier is given by:

$$A_v = g_m \left(\frac{R_C \parallel R_L}{R_S}\right)\left[\left(\frac{r_\pi}{1+\beta}\right) \parallel R_E \parallel R_S\right]$$

Where the symbols enjoy their usual significances.

10

7.

(a) What do you understand by differential signal?

(b) Draw and explain the large signal characteristics of a differential amplifier circuit.

2+8

MODULE 4

8. Draw the diagram of a two-stage common emitter amplifier circuit which exhibits current-shunt feedback. Hence calculate the expression of feedback factor and current gain with feedback.

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MODULE 5

9. Draw the diagram of an RC phase-shift oscillator circuit. Calculate its oscillation frequency.

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