Ref. No.: Ex/IEE/PE/B/T/315B/2025

B. INS. & ELEC. ENGINEERING 3RD YEAR 1ST SEMESTER EXAMINATION 2025

ANALOG MOS CIRCUIT DESIGN

TIME: 3 HOURS **FULL MARKS: 100**

List of Course Outcomes (CO):

CO1: Classify and analyze different types of MOS amplifiers (K4, A1-recognize)

CO2: Explain and interpret the importance of differential amplifiers (K3, A1)

CO3: Describe and explain the behavior of current mirrors (K2, A1)

CO4: Explain and analyze the frequency response of MOS amplifiers (K4, A1)

Instructions to the Examinees:

- Each module is mapped with the corresponding CO
- Attempt questions from **ALL** the modules
- Alternative questions exist within a module, not across the modules
- Different parts of same question should be answered together
- Unless otherwise stated, use the device data shown in Table I and assume $V_{DD} = 3\ V$ where necessary

Table I

Symbol	Value	Unit
$V_{th,n}$	0.7	V
$V_{th,p}$	−0.8	V
γ_n	0.45	$V^{1/2}$
γ_p	0.4	$V^{1/2}$
$\mu_n C_{ox}$	50	$\mu A/V^2$
$\mu_p C_{ox}$	25	$\mu A/V^2$
λ_n	0.1	V^{-1}
λ_p	0.2	V^{-1}

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MODULE 1

ATTEMPT **Q. NO. 1** AND ANY **THREE** FROM THE REST

1. (a) Terminal voltages for the MOS below at G, D, S and B are given by 0.8 V, 0.9 V, 0.1 V and 0 V respectively. Which one of the following is correct?

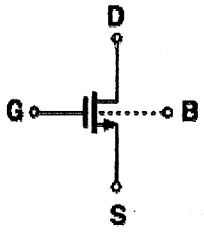

Fig. 1 (a)

(i) MOS is OFF
(ii) MOS is ON and at triode region
(iii) MOS is ON and at saturation region
(iv) Insufficient data

(b) Following circuit is an example of

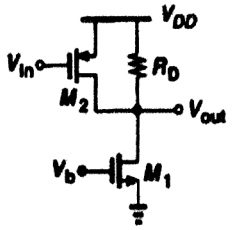

Fig. 1 (b)

(i) CS stage
(ii) CD stage
(iii) CG stage
(iv) Cascode stage

(c) The following circuit will work as CS stage with triode load, provided the value of V_b is

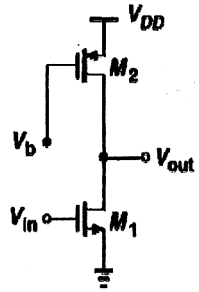

Fig. 1 (c)

(i) Sufficiently low
(ii) Moderate
(iii) Sufficiently large
(iv) Equal to the threshold voltage

(d) Consider the following statements: A) Diode connected load always suffers from body effect B) Diode connected load never suffers from body effect C) CS stage with diode connected load limits the output voltage swing D) CS stage with diode connected load does not limit the output voltage swing. Choose the correct option:

(i) A and C
(ii) A and D
(iii) B and D
(iv) C only

(e) Assuming $\lambda \neq 0, \gamma \neq 0$, output resistance of a source follower circuit is given by:

(i) $\frac{1}{g_m}$

(ii) $\frac{1}{g_{mb}}$

(iii) $\frac{1}{g_m} \| \frac{1}{g_{mb}}$

(iv) $\frac{1}{g_m} \| \frac{1}{g_{mb}} \| r_o$

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2. On which factors, does the trans-conductance of a MOSFET depend? Illustrate these dependences using appropriate graphs. For the arrangement shown in Fig. 2, plot the trans-conductance as a function of V_{DS}.

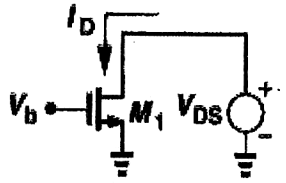


Fig. 2

3+6+6

3. What do you mean by body effect? Synthesize the small signal model of an n-MOS which experiences body effect. Find out the resistance of a diode-connected device. Sketch the variation of g_m and g_{mb} in Fig. 3 as the bias current I_1 increases from 0 to some positive value.

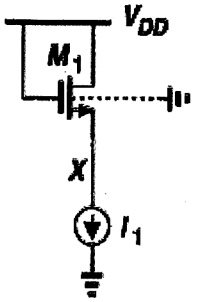


Fig. 3

3+5+3+4

4. Draw and explain the large signal behavior of the circuit in Fig. 4. Hence, calculate its small signal voltage gain. What are the limitations you may face to increase its voltage gain? How can you overcome these limitations?

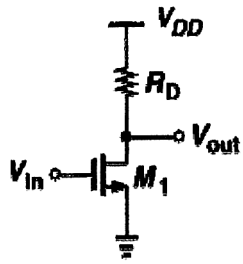


Fig. 4

5+4+3+3

5. Implement one degenerated current source using MOS devices. Hence, find out its equivalent resistance using small signal model. Assuming $\lambda \neq 0$ and $\gamma = 0$, calculate the small signal voltage gain of the circuit shown in Fig. 5.

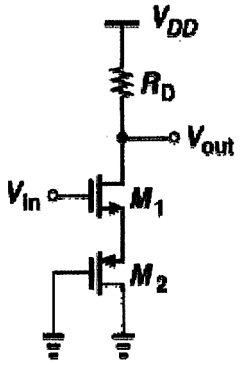
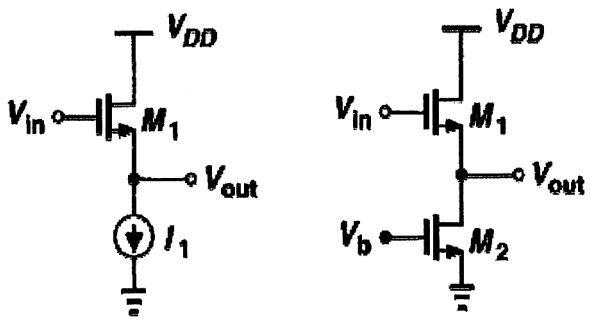


Fig. 5

3+5+7

6. Draw and explain the transfer characteristics of a source follower circuit. Suppose in the circuit of Fig. 6(a), $\left(\frac{W}{L}\right)_1 = 40, I_1 = 200\ \mu A, V_{th,0} = 0.6\ V, 2\varphi_F = 0.7\ V$. Calculate v_{out} for $v_{in} = 1.2\ V$. If I_1 is implemented as M_2 in Fig. 6(b), find the minimum value of $\left(\frac{W}{L}\right)_2$ for which M_2 remains saturated.



(a) **(b)**

Fig. 6

5+10

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MODULE 2

ATTEMPT **Q. NO. 9** AND ANY **ONE** FROM THE REST

7. Show that the equivalent trans-conductance of a symmetric differential amplifier is given by:

$$G_m = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta v_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta v_{in}^2}}$$

,where the symbols enjoy their usual significances.

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8. Find out the differential gain of an assymetric differential amplifier with unequal tranns-conducatnce and non-ideal tail current source.

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9. Explain the reason of using two MOS devices as a load in each half of the circuit in Fig. 7. Assuming $I_{SS} = 1\,mA$ and $\frac{W}{L} = 100$ for all the transistors, determine the voltage gain and calculate V_b such that $I_{D5} = I_{D6} = 0.8(\frac{I_{SS}}{2})$.

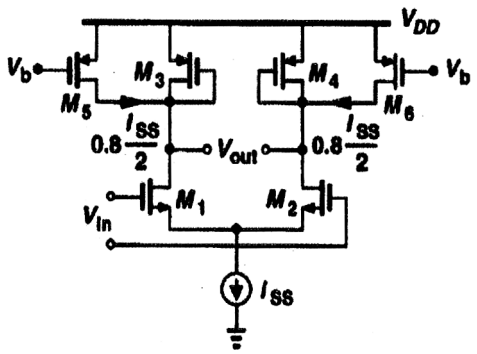

Fig. 7

5+10

MODULE 3

10. Draw and explain the operation of a cascode current mirror circuit. Hence, illustrate on accuracy-voltage headroom trade-off in the design

Or

Show that the common-mode gain of the circuit in Fig. 8 with g_m mismatch is approximately given by:

$$\frac{\Delta V_{out}}{\Delta V_{in,CM}} \approx \frac{(g_{m1} - g_{m2})r_{o3} - \left(\frac{g_{m2}}{g_{m3}}\right)}{1 + (g_{m1} + g_{m2})R_{SS}}$$

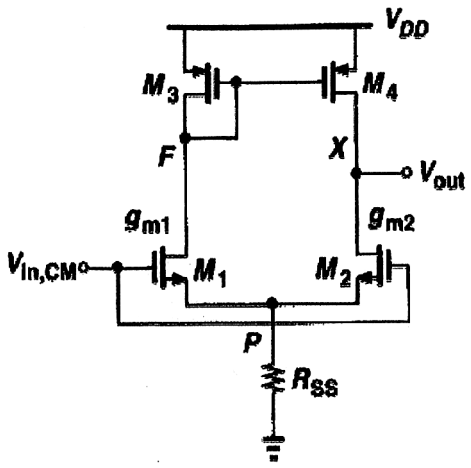

Fig. 8

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MODULE 4

11. One CS stage with resistive load is designed with $\frac{W}{L} = 100, R_S = 1\ K\Omega$ and $R_D = 2\ K\Omega$. Considering the DC drain current to be 1 mA, determine the poles and zero of the circuit.

Or

Find out the transfer function of the circuit shown in Fig. 9 below.

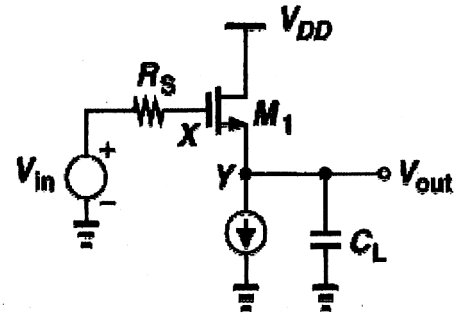

Fig. 9

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