Ref. No.: Ex/IEE/PE/B/T414B/2025

Name of the Examination: B. E. INSTRUMENTATION AND ELECTRONICS ENGINEERING FOURTH YEAR FIRST SEMESTER-2025

Subject: VLSI Design **Time: 3hrs** **Full Marks:100**

Candidates are instructed the answer should be brief and to the point

Group-A (55 marks)

Question No.1 is Compulsory and Answer any **Five** of the following Questions :- **15+(8X5)**

1. a) What is ASIC? Mention its two features. **[CO1/K1]**

b) What is the full from of SSI and how many gates are include in the SSI technology? **[CO1/K1]**

c)_____no of CMOS transistors needed to implement the XOR gate circuit.**(Fill in the blanks)** **[CO3/K2]**

d) In the following device which one is highest mobility**(choose the correct answer)** **[CO1/K1]**

i) NMOS ii) PMOS iii) CMOS iv) Bi-CMOS

e) What is the lithography process in IC design. **[CO2/K2]**

f) How many type of semi custom based ASIC is applicable and explain briefly. **[CO1/K1]**

g)Which method is more complex **(Choose the correct answer)** **[CO4/K3]**

i) Stuck at fault ii) CA iii) combinational ATPG iv) Sequential ATPG

h) What is the design synthesis of IC. **[CO4/K2]**

i) What is automatic Test pattern Generator in VLSI design **[CO4/K2]**

[2+2+1+1+2+2+1+2+2]

2. a) Explain the working principle of Enhancement type NMOS . **[CO1/K2]**

b)What is current mirror? Explain it with a proper diagram. **[CO3/K2]** **[4+(1+3)]**

3. a) Describe the Voltage Transfer Characteristics (VTC) curve of CMOS inverter with the help of neat diagram with necessary input and output voltages. **[CO2/K2]**

b)Explain about MOSFET capacitor? **[CO1/K1]** **[(3+2)+3]**

4. a)Design a NOR with CMOS logic. **[CO3/K2]**

b) Draw the Bi-CMOS of inverter circuit. **[CO3/K2]** **[4+4]**

5. a) Draw the following Boolean expression using CMOS circuit: **[CO2/K1]**

F(A,B,C)=(AB'+BC+AC')

b)What is Pseudo NMOS ? **[CO1/K1]** **[5+3]**

6.Explain and briefly describe the different steps of Fabrication and layout of CMOS circuit.What is the noise margin of CMOS inverter circuit. **[CO3/K1]** **[3+2+3]**

7. Design and explain conventional CMOS full adder circuit. Draw the block diagram of analog signal processing. **[CO2/K2]** **[5+3]**

8.Explain the Characteristics of NMOS Resistive load Inverter circuit also calculate the V_{OH} and V_{OL} **[CO3/K3]** **[2+3+3]**

9.Write down and explain the behavioral style modelling of Half adder circuit using VHDL programming. **[CO4/K3]** **[4+4]**

Group-B (45 Marks)

Answer any **three** from the following question:- **15x3=45**

10.a) What is CMOS λ based design rule. **[CO3/K2]**

b) Explain the P-well CMOS inverter with the help of Stick diagram.**[CO3/K3]**

c) Describe the sheet Resistance to MOS transistor inverter circuit.**(CO3/K2)** **[4+4+7]**

11. a) Draw and Explain the NAND gate structure using Bi-CMOS and stick diagram also. **[CO3/K3]**

b)Explain the switching logic arrangement transistor gates. **[CO3/K2]** **[10+5]**

12. a)Write down some properties of Pass Transistors. **[CO3/K1]**

b) Draw and explain the scaled NMOS Transistor with a neat diagram along with the scaling factors. **[CO3/K1]** **[6+(7+2)]**

13. a) Make a comparative study PLD and FPGA with neat diagram. **[CO3/K1]**

b) Write down the flow chart of fabrication of CMOS n-well process.**[CO2/K1]**

c) Explain the CMOS inverter layout design. **[CO2/K2]** **[5+5+5]**

14. a)Explain a realistic VLSI realization process in fault detection. **[CO4/K3]**

b) Describe the different faults in logic circuit. **[CO4/K2]** **[8+7]**

15. a)Explain the working principle of CMOS differential amplifier. **[CO3/K2]**

b) Make a comparative study among the SSI,MSI,LSI,VLSI technology and their features.**[CO1/K1]** **[9+6]**
