[**CO5 : Microprocessor**]

9. *(a)* Write names and sizes of user accessible registers of 8085 μP. What are the functions of flag register?

(b) Explain what happens on execution of the instructions MOV B, C and MOV D, M. 4+4

10. *(a)* What are the essential connections of a memory chip?

(b) Draw a schematic diagram of memory chip connection with μP and explain what signals μP generate to read a data byte from memory. 3+5

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B. Sc. EXAMINATION, 2024

(2nd Year, 1st Semester)

PHYSICS (HONOURS)

PAPER – CORE 7

(Digital Systems and Applications)

Time : *Two Hours* *Full Marks* : 40

Answer any ***one*** question from each **CO**

[**CO1 : Number system & Logic Gates**]

1. *(a)* Convert decimal number $12\frac{3}{32}$ to binary. [Hint : Express the number in hexadecimal, taking the denominator of the fractional part of the number in power of 16]

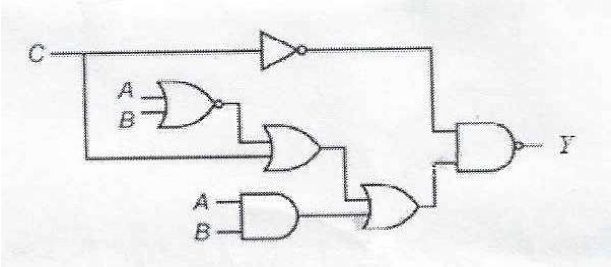
(b) Consider the $(123)_5 = (X8)_Y$ is a correct equation where X and Y are unknown. Find the possible solutions for X and Y and show that number at RHS of equation may be a decimal number.

(c) Subtract the hexadecimal number 4A0E.A9 from 67F2.6E using 2's compliment arithmetic and represent the results in sign magnitude binary number format.

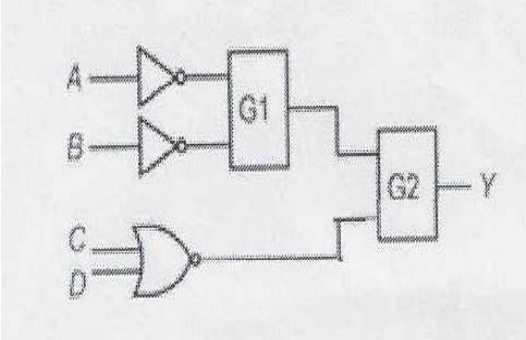
(d) Draw the circuit diagram of 2-input NOR gate. 2+2+2+2

2. *(a)* Add the hexadecimal numbers 4A0E.A9 and 67F2.6E. Write down the result in binary format.

(b) Show that the circuit given below represent basic logic gate if C = 0.



(c) In the circuit shown in figure below, the output is required to be $Y = AB + \overline{C}\overline{D}$. What are the gates G1 and G2 must be?



(b) Draw a logic circuit using SR flip-flop (FF) where $S = J\overline{Q}n$ and R = KQ_n, J and K are two external input. Write down the characteristic table of the circuit and show that it will act as a JK FF. 5+3

[**CO4 : Sequential logic circuit**]

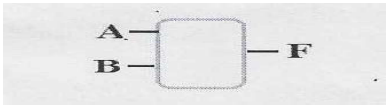
7. *(a)* Draw circuit diagram of a 3 bit ripple counter using negative edge triggered JK-flip-flop. Explain its count sequence for a complete count period and also show timing diagrams. What is the main disadvantage of a ripple counter?

(b) Suppose by some connection error in the above circuit for the middle flip flop Q and Q′ have been exchanged. Write out the count sequence for this circuit. 5+3

8. *(a)* Draw the circuit diagram of a Parallel In Serial Out (PISO) shift register and explain its operation.

(b) A 4-bit shift register circuit is converted into a counter by connecting $\overline{Q}$ of last flip-flop to its input. Write its count sequence. 4+4

(d) The output of the logic gate given in figure below is $F(A, B) = \overline{A}B$. Design a two input NAND gate using this gate.



2+2+2+2

[CO2 : Boolean algebra & Karnaugh map]

3. *(a)* Explain whether the NAND operation is commutative and associative or not. Design a 3 input NAND using 2 input NAND gates.

(b) Reduce the Boolean expression $\overline{\overline{ABC}(A+B)+BC}$ in minimal form.

(c) Implement the function

$F(A,B,C,D) = \overline{A}\overline{B}\overline{C} + A\overline{B}D + \overline{A}\overline{B}C\overline{D};\ d = ABC + A\overline{B}\overline{D}$

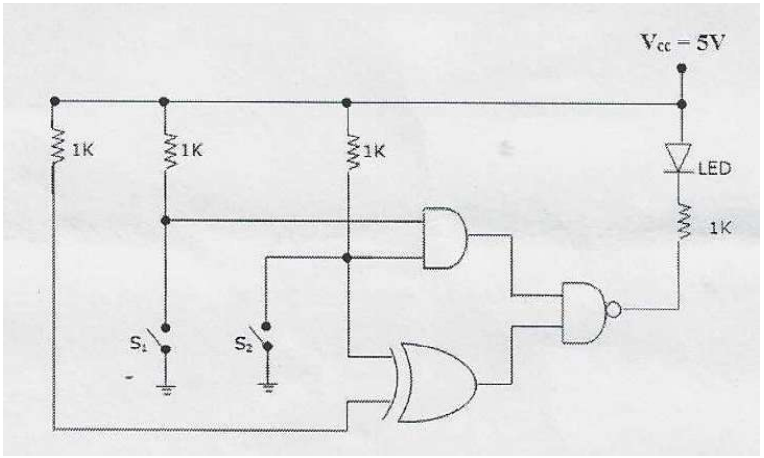
using all NAND gates. 3+2+3

4. *(a)* If the Boolean function $Z = PQ + PQR + PQRS + PQRST + PQRSTU$, then find $\overline{Z}$ in minimal form.

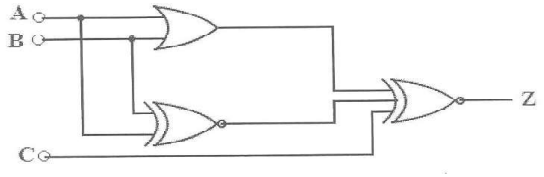
(b) The four variable function F is given as : F (A B C D) = $\sum$m (2, 3, 8, 10, 11, 12, 14, 15). Reduce F in SOP, POS, NAND and NOR formats and realize it using NOR gates. 2+6

[CO3 : Combinational logic circuit & flip flop]

5. *(a)* Show that in circuit given below the LED should not glow irrespective of switch position.



(b) Find the required input conditions (A, B, C) for which the output of the logic circuit shown in figure below will be Z = 1.



4+4

6. *(a)* What is multiplexer (MUX)? Write down the job supposed to be executed by a 4 to 1 line MUX and hence obtain the truth table and determine the logic expression for its outputs. Draw its circuit diagram.