Design of On-Chip CMOS Low-Drop Out Voltage regulator

Thesis submitted in partial fulfilment of the requirements for the degree

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Master of Engineering

in

Electronics and Tele-Communication Engineering

by

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DECLARATION

I hereby declare that this thesis entitled **"Design of On-Chip CMOS Low-Drop Out Voltage regulator"** contains a literature survey and original research work by the undersigned, as part of my degree of **Master of Engineering in Electronics and Tele-Communication Engineering**, with specialization in **Electron Device**.

All information has been obtained and presented in accordance with academic rules and ethical conduct.

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Abstract

Low dropout (LDO) voltage regulators are commonly used to power low-voltage digital circuits such as microprocessor cores. These digital circuits are typically constantly changing from one operating mode to another. Therefore, the load demands can change rapidly, resulting in large voltage spikes at the regulator's output that can adversely affect the digital circuitry

Low dropout (LDO) voltage regulators are commonly used to power low-voltage digital circuits such as microprocessor cores. These digital circuits are typically constantly changing from one operating mode to another. Therefore, the load demands can change rapidly, resulting in large voltage spikes at the regulator's output that can adversely affect the digital circuitry. The main challenge in developing this type of regulator is to reduce quiescent current and achieve high current efficiency while ensuring good stability response and control performance. Therefore, various circuit techniques must be carefully added to compensate for the lack of large external capacitors and minimize the impact on system efficiency.

This thesis focuses on developing a fully integrated low-dropout regulator with excellent dynamic performance, high regulation performance, and extremely low power consumption.

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Signature of Candidate

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Chapter 1

Introduction

Two trends characterize the semiconductor industry and consumer electronics in recent years: the reduction of project area and power consumption. These two requirements require integrated electronic silicon systems with increasingly low power consumption and maximum integration that allow the elimination of external components on the chip (system-on-chip paradigm or SoC). To achieve this, different optimized voltage ranges must be generated internally for different integration functions with the required performance and consumption levels. It is therefore increasingly necessary to consider in detail which current and voltage converters should be integrated on the chip (on-chip) and which should remain outside the chip (off-chip). It is also important to decide what type of circuits are required for each voltage range: linear circuits (linear regulators, linear regulators LDOs, output devices PMOS or NMOS, etc.) or switching circuits (switching capacitors, switching inductors). Similarly, a control system with a particular feedback network needs to be designed based on the output voltage specification and the frequency compensation method to ensure its stability.

1.1 Motivation

Technology is moving fast Because of this, there's a growing need for power management solutions that are smaller, more efficient, & really reliable. As our electronic devices keep shrinking and becoming more integrated, we face some tricky problems with traditional power supply parts. For example, Low-Dropout (LDO) regulators usually need big external capacitors. These capacitors take up precious space on printed circuit boards (PCBs). Plus, they can add extra costs and make designs more complicated. In this thesis, we dive into exploring capacitor-less LDO (CL-LDO) regulators. The goal to tackle these challenges head-on by getting rid of those bulky external capacitors, we can still keep high performance & stability.

1.2 Objective

The objective of this thesis is to design, develop, and evaluate a fully integrated Capacitor-Less Low-Dropout (CL- LDO) regulator that achieves high performance in terms of stability, dynamic response, and power efficiency, without the need for large external capacitors. This work aims to address the challenges and limitations of conventional LDO regulators by exploring innovative circuit techniques and compensation strategies. The LDO must be fully integrated on-chip, which means that no external capacitor can be used to set the dominant pole and to avoid output voltage changes during load current transitions. This makes the design particularly challenging, especially when compared to conventional LDO solutions with external capacitors.

Chapter 2

Preliminary design of LDO and literature survey:

2.1 Basics of LDO

Figure 2.1 shows a classic CMOS low dropout architecture. It consists of an error amplifier (EA), a feedback resistor network, a pass transistor, and a reference voltage. The error amplifier is responsible for comparing the reference voltage with the output voltage obtained by the resistor feedback and driving the pass transistor accordingly. If the regulator has a large enough voltage gain, the output voltage is determined by the ratio of the output resistors R1 and R2 and the voltage reference.

$$V_{out} = (1 + \frac{R_1}{R_2})V_{Ref} \qquad (2.1)$$

The pass transistor is a power device that controls the current flowing to the load. This structure has two low frequency poles located at the output of the LDO and the output of the error amplifier, respectively, that must be compensated. To produce a large output current without a large voltage drop, the power transistor must be very large compared to the internal transistors. Therefore, the equivalent parasitic capacitance at the gate of the power transistor is relatively large. Traditional LDOs use large external capacitors to create the dominant pole. Additionally, it provides instantaneous charging during fast load transients [1].

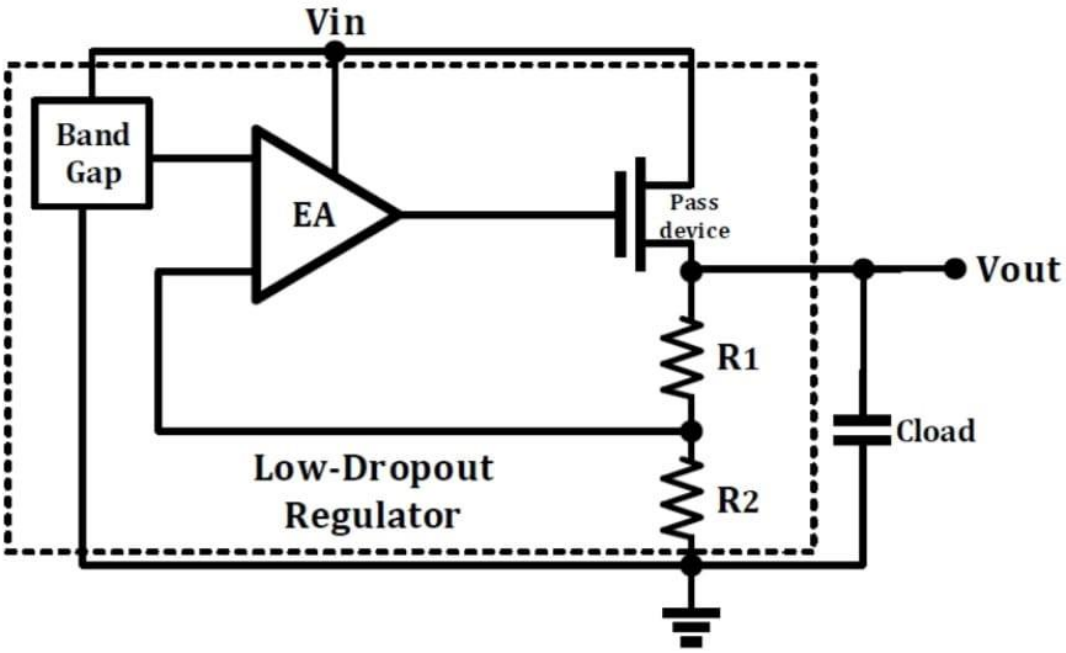


Figure 2.1: Linear voltage regulator

2.2 LDO Structure

LDO regulators are essential components in modern electronics, providing stable and regulated output voltages. The structure of an LDO involves key components like the pass element, error amplifier, reference voltage, feedback network, and output capacitor. Different LDO structures cater to various application requirements, from basic designs to advanced configurations optimized for low quiescent current, high PSRR, and rapid transient response. Understanding these structures and their design considerations is crucial for selecting and designing effective LDO regulators for specific applications.

1. Pass element
2. Error amplifier
3. Reference voltage
4. Output capacitor
5. Feedback loop

2.2.1 Pass element

The output stage of a linear regulator can be designed in various possible configurations depending on the circuit performance and energy efficiency. An important criterion for selecting a pass-through device is the dropout voltage from the input voltage to the output voltage. The different pass device topologies used in CMOS linear regulators, namely NMOS source follower, PMOS common source. In general, NMOS transistors of the same size have higher current conduction due to higher electron mobility. However, to achieve a lower dropout voltage, PMOS is preferred despite its lower current conduction. Also, its gate voltage is always lower than the supply voltage. In contrast, for an NMOS, if it is designed to operate at a low dropout voltage, the gate voltage will be higher than the supply voltage. Therefore, additional circuitry may be required, making the design more complex. However, NMOS consumes less area for the same maximum current and provides better dynamic performance for large signals because its source node is directly connected to the regulator's output. Therefore, if the load current suddenly changes, for example, from $I_{L_{min}}$ to $I_{L_{max}}$, V_{out} decreases and V_{gs} increases rapidly, adjusting the pass device to drive $I_{L_{max}}$.

On the other hand the combination of lower $R_{ds_{on}}$ and ability to operate with negative V_{gs} makes PMOS transistors more suitable for LDO application. DC gain is also affected by the architecture of the pass device. With pMOS, it acts as a second stage (common source), thus increasing the overall gain and providing better steady-state control, as will be discussed later in this chapter. With NMOS, DC gain is ideally unaffected, as it acts as a common drain, and instead has a much lower output resistance, making it easier to stabilize the regulator.[2]

2.2.1 Error amplifier

The error amplifier (EA) compares the reference voltage with the feedback voltage from the output and amplifies the difference [3]. It is responsible of driving the gate of the pass device to the appropriate operating point to ensure that the output is at the correct voltage [4]. As the current load and the power supply changes, the EA drives the pass device to maintain a constant output voltage. Therefore, the error amplifier design is crucial to ensure the driving requirements of the pass device and the performance of the system.

The main designs considerations of the error amplifier is High DC gain to ensure good line and load regulations, High bandwidth and high output current slew rate for responding to fast load transitions Large output voltage swing for driving the pass devices under the whole current load and input voltage range, The topology is directly related to the overall power-supply rejection of the regulator.

2.2.2 Reference voltage

In a LDO regulator, reference voltage is a stable and voltage used to compare and regulate the output voltage [5]. It acts as the benchmark for the error amplifier, which modulates the pass element to achieve the target output voltage. The reference voltage is usually produced by a band-gap reference circuit, which is renowned for its stability across fluctuations in temperature, supply voltage and manufacturing variations.

2.2.3 Output capacitor

In LDO the output capacitor plays a very crucial role. It helps to maintain the transient response as well as stability. The output and parasitic poles move whenever load variation occurs. [6] So it is not easy to maintain a stable system when the pole moves with the load. It also helps to maintain PSRR high at high frequency.

The output capacitor is essential for the stability of the LDO regulator. It helps maintain a stable output voltage by providing a local energy reservoir that can supply or absorb current during transient events. During sudden changes in load (transient events), the output capacitor provides immediate current to the load or absorbs excess current, reducing voltage spikes (overshoot and undershoot) and improving the transient response. The output capacitor helps filter out high-frequency noise from the output voltage, ensuring a clean and stable voltage supply to the load. By stabilizing the output voltage, the output capacitor aids in maintaining the accuracy of the LDO regulator, especially under varying load conditions. The value of the output capacitor is typically specified by the LDO manufacturer. It needs to be within a certain range to ensure stability and optimal performance.

2.2.4 Feedback loop

The feedback loop in an LDO regulator is fundamental to its ability to maintain a stable and precise output voltage. By continuously comparing the output voltage to a reference voltage and adjusting the pass element accordingly, the feedback loop ensures that the LDO can handle variations in input voltage and load current, providing reliable power to electronic circuits. Stability and response time are critical considerations in the design of the feedback loop to ensure optimal performance. A negative feedback system is used to regulate the output voltage, which consists of two resistors. It is crucial to know that if the pass element is PMOS, we connect the feedback signal to the positive terminal of the error amplifier and if the pass element is NMOS, we connect the feedback signal to the negative terminal of the error amplifier to achieve a negative feedback loop. [7]

2.3 Parameters of LDO Regulators

There are some design specifications to evaluate the regulator performance in steady state and transient state.

2.3.1 Dropout voltage

Dropout voltage is the difference between input voltage and output voltage. V_{drop} is a crucial parameter to maintain high efficiency, low power dissipation and stable output.

$$V_{drop} = V_{in} - V_{out} \qquad (2.2)$$

If V_{drop} is very less, then the power transistor operates as a switch which provides very low loop gain and it is challenging to make regulated V_{out}. V_{drop} also depends on maximum load current and on resistance of the Power Transistor.

$$V_{drop} = I_{load} . R_{DS_{on}} \qquad (2.3)$$

Reducing the dropout voltage of a Low Dropout (LDO) regulator is critical for enhancing its efficiency and performance, especially in battery-powered applications. A method used to achieve a lower dropout voltage is to choose pass elements with low on-resistance ($R_{DS_{on}}$). Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs), especially PMOS transistors, are commonly used because

they offer lower resistance compared to bipolar junction transistors (BJTs), and dropout voltage can increase with higher load currents because the voltage drop across the pass element increases with current. Dropout voltage also affected by the quiescent current for reducing dropout voltage require design techniques that minimize the current consumed by the internal circuitry, thus allowing more current to be available for the load, effectively reducing the dropout voltage.

2.3.2 Efficiency

Efficiency is a very important parameter especially in portable systems since it determines the life time battery. The power efficiency of LDO is the relationship between the output power and the power supply which is defined by the drop-out voltage, the load current, and the quiescent current. The relationship is shown in equations 2.4.

$$\eta = \frac{V_{out} \cdot I_{load}}{V_{in} \cdot (I_{load} + I_q)} \qquad (2.4)$$

Where VIN and VOUT are input and output voltages, respectively. I_q is the quiescent current and ILOAD the load current. Two different situations can be identified for the analysis of power efficiency, one related to small load currents 3 and the other to large load currents2.4. Assuming $V_{out} \approx V_{in}$, the relation reduces to equation 3 for small load current conditions (I_{load}), thus the power efficiency is determined by the quiescent current itself. For portable devices this parameter is extremely important since if the current load is very low the longevity of the battery life will depend exclusively on the quiescent current consumed.

$$\eta_{lightload} \approx \frac{I_{load}}{I_{load} + I_q} \qquad (2.5)$$

$$\eta_{hevyload} \approx \frac{V_{out}}{V_{in}} \qquad (2.6)$$

In high load current condition the quiescent current is negligible compared with load current.

2.3.3 Power supply rejection ratio

PSRR refers to the power supply rejection ratio or ripple rejection ratio. The ratio of input ripple to the output ripple is called PSRR. It is also frequency- dependent. While maintaining a constant difference in the voltages (V_g and V_s), the output voltage is free of ripple if the ripple on the gate voltage (VG) of the Pass Transistor is equal to the ripple on input side VIN ($V_{inripple}$). In this case, the Pass transistor does not pass any ripple current to the output due to the $V_{inripple}$.

$$\text{PSRR} = 20\log\left(\frac{V_{inripple}}{V_{outripple}}\right) \qquad (2.7)$$

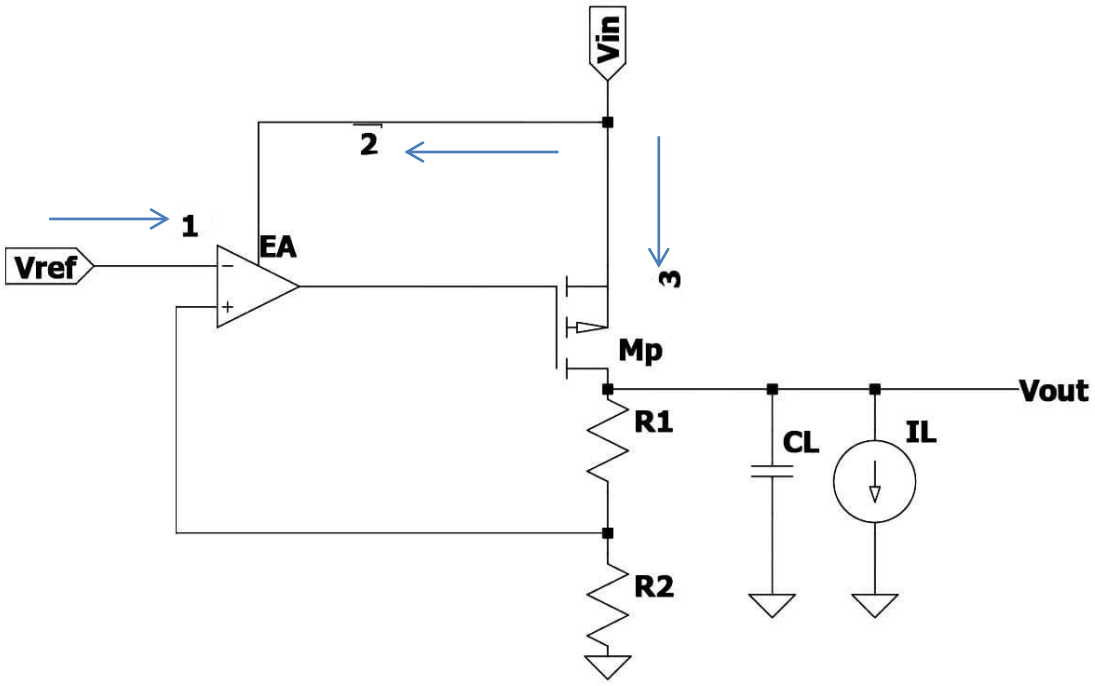


Figure2.2: Basic LDO circuit [10]

As shown in fig 2 the noise coming from the input supply can couple to the output through several paths through the voltage reference, the error amplifier and the pass device MP. The contribution of supply noise coming from the path 1 usually is negligible. The ripple is mnimum, if a high PSRR achieved by choosing proper voltage

reference. Otherwise, it can be easily reduced by adding a low pass filter to the output of the voltage reference. Basically, the PSRR of the LDO strongly depends on the error amplifier and the pass devices topologies.

The concept to define the error amplifiers as Type – A and Type - B was introduced in[8] order to analyze the PSRR of the LDO. This concept is only valid for DC and low frequencies PSRR. For high frequencies, the analysis are no longer valid, since it does not take into account the parasitics paths. However, it is useful to gain insight how the error amplifier architecture can affect the performance of the regulator in terms of PSRR. Fig.2.3 show an example of a Type-A amplifier and the small-signal model for PSR of Type-A amplifiers. The Type-A consists of an PMOS input differential pair and a PMOS current mirror load. The model is obtained by applying an AC signal at the power supply V in and grounding the inputs of the amplifier V + and V −. R2 is the channel resistance of transistor M2, and R1 is the equivalent degenerated resistance, which is approximately equal to gm_{M_1}, rds_{M_1}, $2R_b$, where resistor I_b represents the current source R_b small signal resistance, gm_{M_1}, and rds_{M_1} are the transconductance and the channel resistance of transistors M1. Assuming R1 ≫ $1/g_m$, the current i_{R_1} can be Approximate to V_{in}/R_1. Equation 2 shows the derivation of the transfer-function V_{outA}/V_{in}. Therefore, for Type-A amplifiers, the supply ripple is ideally transferred to the output.

$$V_{out_A} = V_{in}\left(\frac{R_1}{R_1+R_2}\right) + i_{R_1}(R_1 \;//\; R_2) \approx V_{in}\left(\frac{R_1}{R_1+R_2}\right) + \frac{V_{in}}{R_1}\left(\frac{R_1R_2}{R_1+R_2}\right) = V_{in} \qquad (2.8)$$

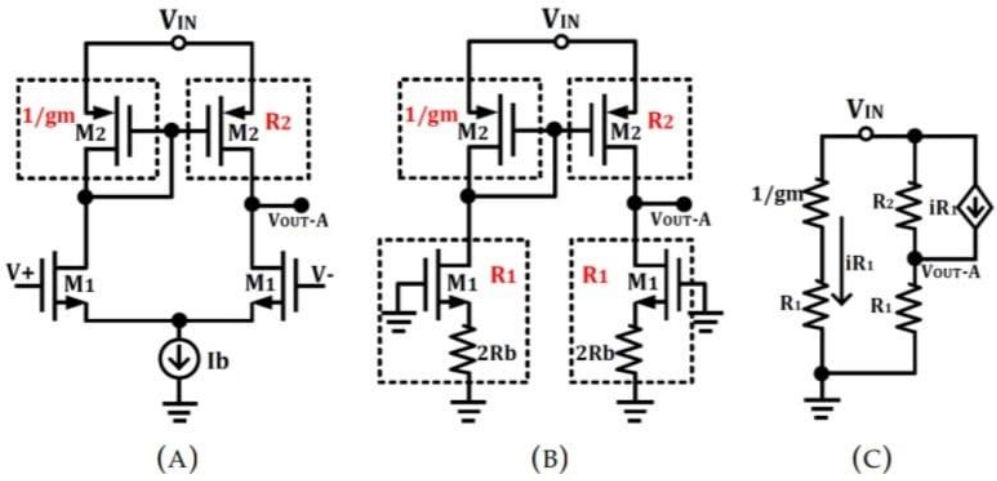


Figure 3: Type A Error amplifier small signal translations [10]

On the other hand, an example of Type-B amplifier and the small signal for PSR of Type - B amplifiers are shown in Fig.4 respectively. The amplifier consists of a PMOS differential input pair and NMOS current mirror. The small-signal is obtained in the same way as Type - A, by applying an AC signal at the power supply V in and grounding the inputs of the amplifier. The derivation of the transfer function V_{out_B}/V_{in} is as follows:

$$V_{out_B} = V_{in}\left(\frac{R_1}{R_1+R_2}\right) - i_{R_1}(R_1 \;//\; R_2) \approx V_{in}\left(\frac{R_1}{R_1+R_2}\right) - \frac{V_{in}}{R_1}\left(\frac{R_1R_2}{R_1+R_2}\right)=0 \qquad (2.9)$$

As can be observed, ideally no AC ripple appears at the output. Thus, the output is isolated from the power supply

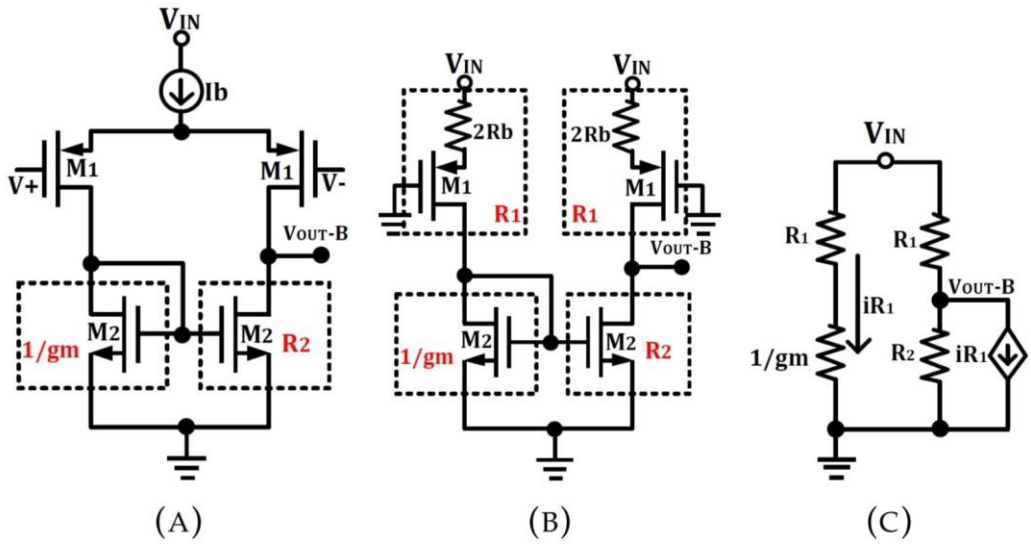


Figure2. 4: Type- B error amplifier small signal translations [10]

pass transistors, as shown in Fig.2.5 c and 2.5 d, the NMOS will conduct the ripple present at its gate directly to the source; the output of the regulator. Therefore, to reduce the ripple at the output, the pass transistor also has an important role in the PSRR. For example, considering NMOS is crucial to design the error amplifier such that the ripple at the gate of the NMOS is the minimum possible (Type-B EA). In other words gate-source (V_{gs}) should be common-mode with respect to each other.

PMOS pass transistors present the opposite scenario (Fig. 2.5a and 2.5b). To eliminate the supply ripple at the output, the gate of the PMOS should present the same ripple (Type-A EA) so that the gate is common-mode with respect to the source.

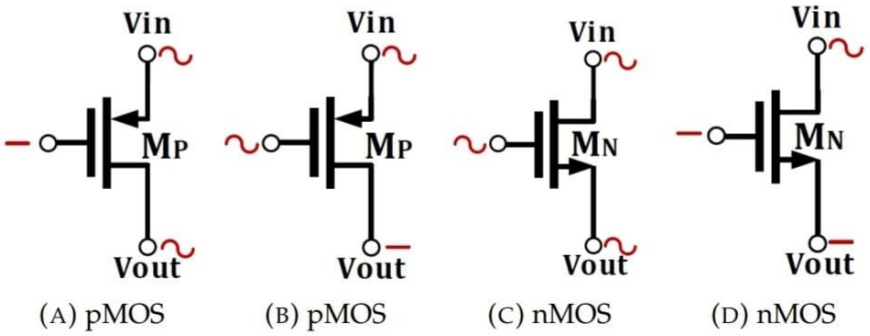


Figure 2.5: Effects of common-mode signals on VOUT

Next table 1 summarizes how PSR is affected depending on what type of error amplifier (Type-A/B) and pass transistor (NMOS/PMOS) are used.

Error amplifier	Pass device	PSR
Type-A	pMOS	Better
Type-A	nMOS	Worse
Type-B	nMOS	Better
Type-B	pMOS	Worse

Table2.1: PSRR depending on error amplifier and pass device topologies.

2.3.4 Regulating performance

The voltage regulator performance can be divided into steady-state regulation and the dynamic regulation. The steady-state regulation is mainly affected by the loop-gain of the LDO. The dynamic performance is the most challenging parameter of the LDO, especially for the capacitor-less which goes without the large output capacitor.

The steady-state parameters include the load regulation and the line regulation. They are normally defined for a given LDO regulator, and measure the capability to regulate the steady-state output voltage for given line and load steady-state values.

Load regulation: The load regulation is the capability of the regulator to maintain the output voltage with steady state variations in load current. It is measured when the output voltage is in steady state. It depends on the LDO output resistance ROL and the LDO open-loop gain ROL.

$$\textit{Load regulation} = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{R_{OL}}{1+A_{OL}R_{OL}} \qquad (2.10)$$

Therefore, a load current change is equivalent to the closed loop output resistance of the regulator thus the higher the DC gain, the better the load regulation.

Line regulation: Line regulation defines the ratio of the output variation change in response to a variation in the input voltage after the regulator has reached the steady state. It depends on the pass device transconductance, g_{mp}.

$$\textit{Line regulation} = \frac{\Delta V_{Out}}{\Delta \mathrm{I}_{Out}} \approx \frac{g_{mp}R_{OL}}{A_{OL}} + \frac{1}{\beta}\left(\frac{\Delta V_{ref}}{\Delta V_{in}}\right) \qquad (2.11)$$

The LDO output resistance ROL, the LDO open-loop gain ROL and the feedback gain β.

2.3.5 Dynamic response

As the main purpose of this thesis is to improve the transient response of the capacitor-less LDOs, the next chapters will constantly mention the concepts presented in the following of this subsection. The dynamic-state specify the ability of the LDO to regulate the output voltage during load transient transitions. Responding

to a load transient becomes challenging when the load current steps are very fast. This is common for digital circuits where clock speeds are high and the circuits have large logical functionalities. Responding to a current change with a rise and fall times of several nanoseconds requires a very fast response (bandwidth) from the regulator which is not achievable for very low quiescent current. Hence, these current transitions are outside of the time response and the regulator cannot react to the load change.

Fig.2.7 illustrates a typical output response to a worst-case load current variation, when the load current suddenly transitions from its highest value to its lower value, and vice versa. The capability of the regulator to respond to these fast current load transitions will depend on the current-load, the output capacitor, and the LDO response time. Where I_{MAX} is the maximum output current, C_{out} is the output capacitor and Δ_{tr} is the regulator response time. As seen, ΔV_{out} is inversely proportional to Cout. Conventional LDO topologies make use of a large capacitor at the output in parallel to the load. The purpose of this large capacitor is to act like a charge source during fast load current transitions and so improve the output voltage change of the regulator in addition to its AC stability.[1]

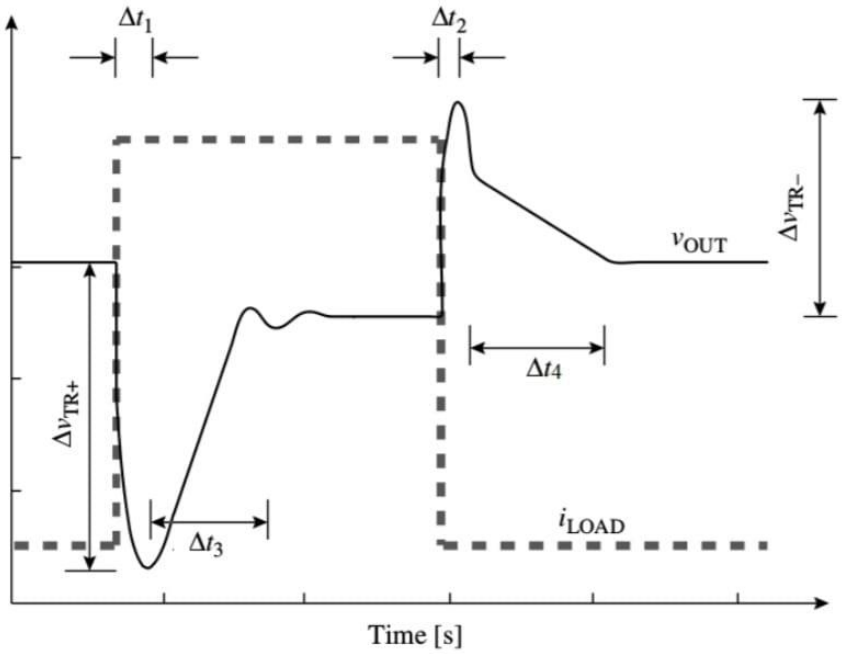


Figure2.6: Transient response to abrupt load current changes [11]

$$\Delta V_{Out} = \frac{I_{MAX}\Delta tr}{C_{Out}} \qquad (2.12)$$

Therefore, they will present better load regulation compared to capacitor-less LDO regulators. The response time Δ_{tr} (Δ_{tr_1},Δ_{tr_2}) is affected by the closed-loop bandwidth and also by the internal slew rate due to the parasitic capacitors which cause slewing effects that degrade the regulator's load response.

$$\Delta tr = t_{BW} + t_{SR} = \frac{2.2}{BW} + C_{pass}\frac{\Delta V_{pass}}{I_{SR}} \qquad (2.13)$$

Where t_{sr} is the slew rate time, 2.2 BW is the bandwidth delay time, C_{pass} is the parasitic capacitance at the gate of the pass device, and I_{SR} is the current driving the C_{pass}. The value of C_{pass} is mainly due to the gate capacitance of the pass device since the transistor is designed to have low voltage drop at maximum load current, i.e the transistor size can be very large, thus capacitance C_{GD} and C_{GS} are usually large. In the case of a positive load current transition (I_{LOAD}suddenly increase), the settling-time (Δtr3) is dependent on the time required for the error amplifier to fully discharge the equivalent capacitance C_{pass} and the phase-margin of the loop frequency response. Usually the settling-time of the overshoot (Δ_{tr_4}) is larger compared to the undershoot. This is mainly because when a fast negative load current step occurs, the regulator takes some time to react (Δ_{tr_2}), and meanwhile the pass device keeps sourcing current which charges the output capacitor CL. Once the regulator responds the pass device stop sourcing current. However, as the output capacitor is charged due to the slowness of the regulator, the output voltage may not return back to its targeted voltage until it does not fully discharge. As a consequence, the settling time would depend on the sinking capabilities the regulator has in order to discharge and slew the output capacitor.

2.3.6 Stability

Since the LDO regulator is based on negative feedback, it is very important to ensure the correct frequency response and closed-loop stability. The locations of the poles and the unity gain bandwidth (UGB) vary significantly with the load current condition.

The compensation strategy would change depending on the size of the output capacitor: In conventional LDO (in fig2.8) the dominant pole (DP) is located at the output node. This is mainly because of the very large external capacitor and the high output impedance. Furthermore, a non-dominant pole is located at the gate of the pass device due to the high output impedance of the error amplifier and the parasitic capacitance C_{gs} and C_{gd} of the pass device. On the other hand, capacitor-less LDO shown in Fig.2.9, has the dominant pole (DP) and non-dominant pole located at the gate of the pass device and the output node, respectively. . In both cases, these two low-frequency poles can be very close together. Therefore, external or internal compensation is required in order to guarantee the stability of both regulators.

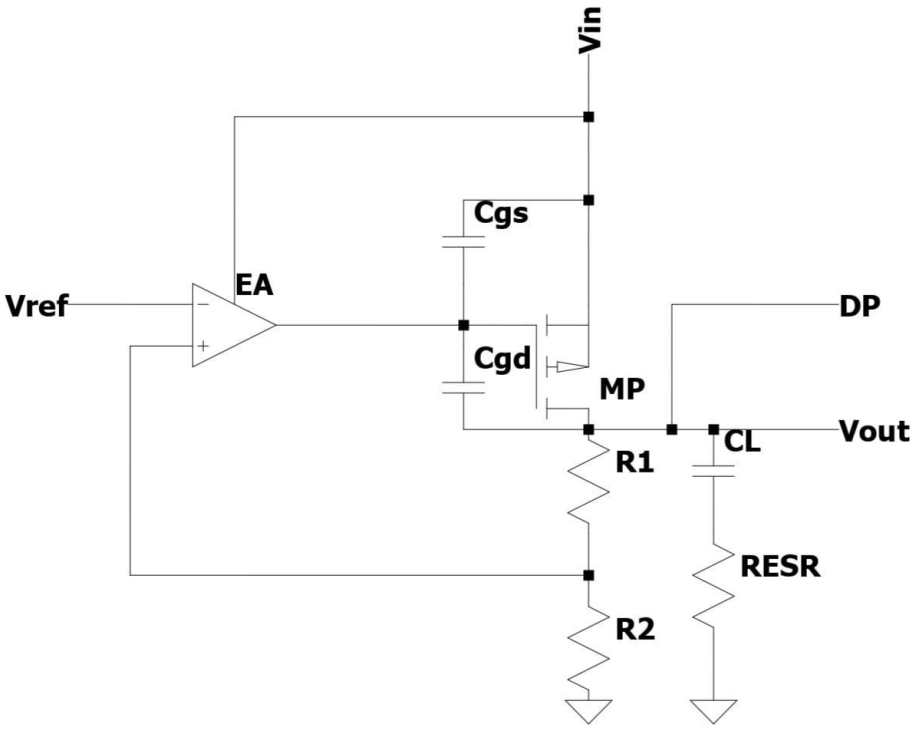


Figure2.7: Conventional LDO regulator

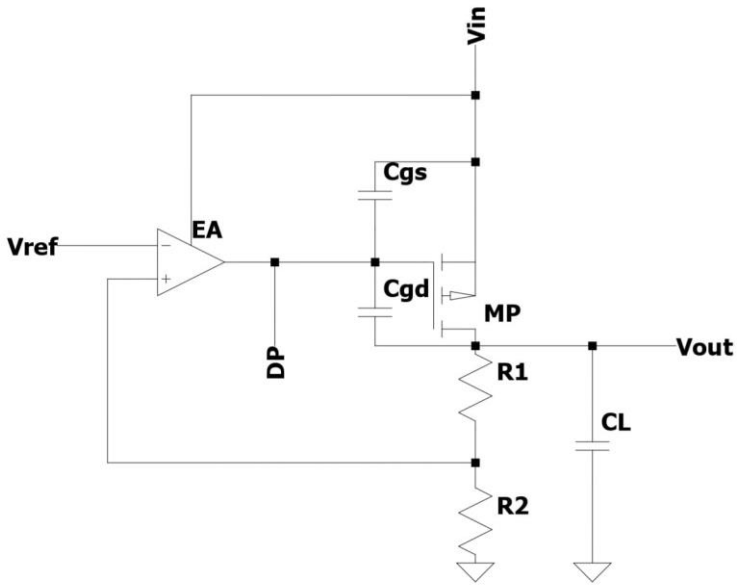


Figure.2.8: Capacitor less LDO regulator (ON CHIP)

Usually, conventional LDO makes use of the equivalent series resistance RESR of the load capacitor to produce a LHP zero for compensating the phase shift introduced by the non-dominant pole [9].

2.4 Literature survey

Low-Dropout (LDO) regulators are integral components in modern electronic systems, offering stable and low-noise power supply solutions. Traditional LDO designs incorporate large output capacitors to ensure stability and transient response. However, the demand for compact, efficient, and integrated power management solutions has spurred research into capacitor-less LDO regulators, which eliminate the need for bulky external capacitors. This literature survey explores the advancements and design strategies in the field of capacitor-less LDO regulators.

In this section the most recent techniques to improve the CL-LDO performance are presented.

2.4.1 Capacitive coupling

The methods discussed in [10][11] address load transient and AC stability issues by utilizing an auxiliary fast loop (differentiator) that includes a current amplifier connected in series with a capacitor Cf as illustrated in Fig. 2.10.

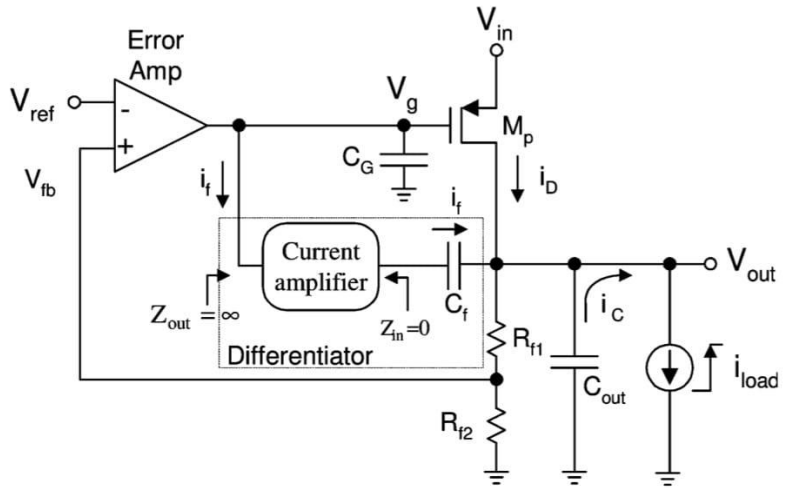


Figure2.9: LDO topology including differentiator [12].

The capacitor Cf reacts to any changes in the output voltage by generating a current. This current is then amplified by the current amplifier and injected into the gate capacitance of the pass device, thereby enhancing the transient response. Additionally, the auxiliary loop helps to split the poles, similar to the approach in [12][13], thereby improving AC stability. However, this technique requires additional capacitors and resistors, leading to an increase in chip area.

2.4.2 Adaptive power transistor

An adaptive power transistor is a circuit technique that enables a regulator to switch between two-stage and three-stage modes based on the current load. During light load conditions, the regulator operates in a two-stage mode, where both the second stage and the main power transistor (MP2) are deactivated, and a smaller sub-power transistor (MP1) functions as the pass device. As the load current increases, the second stage, which also acts as a current comparator, activates MP2 to deliver current to the output, transitioning the regulator to a three-stage mode. This transition enhances the gain of the closed-loop low dropout (CL-LDO) regulator, thereby improving load and line regulation, as indicated by equations 7 and 8.

Switching between two-stage and three-stage modes based on the load current optimizes load and line regulation without causing stability issues. Additionally, since MP1 is designed for light current loads, it can be much smaller than MP2. This significantly reduces the equivalent gate capacitance at the gate of the pass device MP1, resulting in a faster time response for driving MP1. This thesis is based on this circuit technique which is presented in [14].

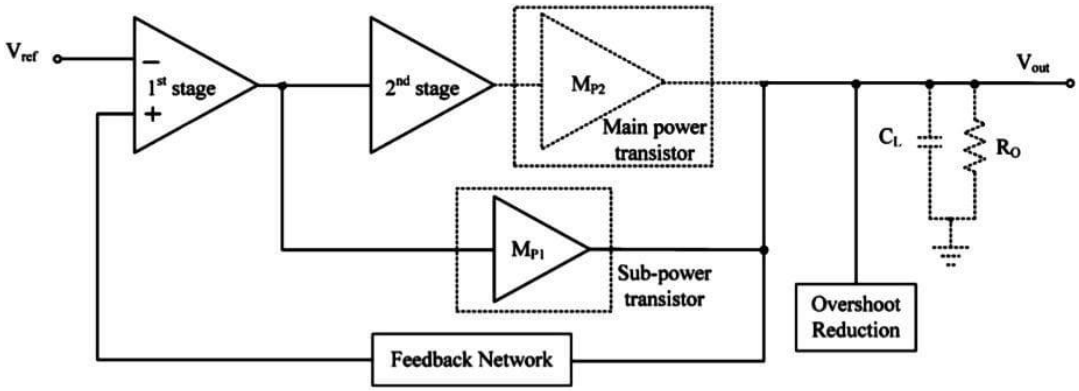


Figure 2.10: Adaptive power transistor architecture [7]

2.4.3 High slew rate error amplifier

The architectures described in references [15, 16] utilize a current-mode error amplifier rather than a voltage-mode amplifier to enhance the transient response. These designs incorporate a Class-AB current-mode transconductance amplifier (CTA) to efficiently sink current.

To source more current for discharging and charging the gate capacitance of the pass device during a load transient transition, a Class-AB current-mode transconductance amplifier (CTA) is employed. When a discrepancy between the reference voltage and the output voltage is detected, the CTA generates a current to either sink or source the gate capacitance of the pass device. However, there is a significant trade-off between AC stability and slew rate. To maintain stability under light load conditions, the transistors that drive the pass device are relatively small, limiting their ability to quickly sink or source the necessary current to adjust the gate voltage of the pass device. This can result in large overshoot and undershoot, which may not meet specifications in some applications.[17]

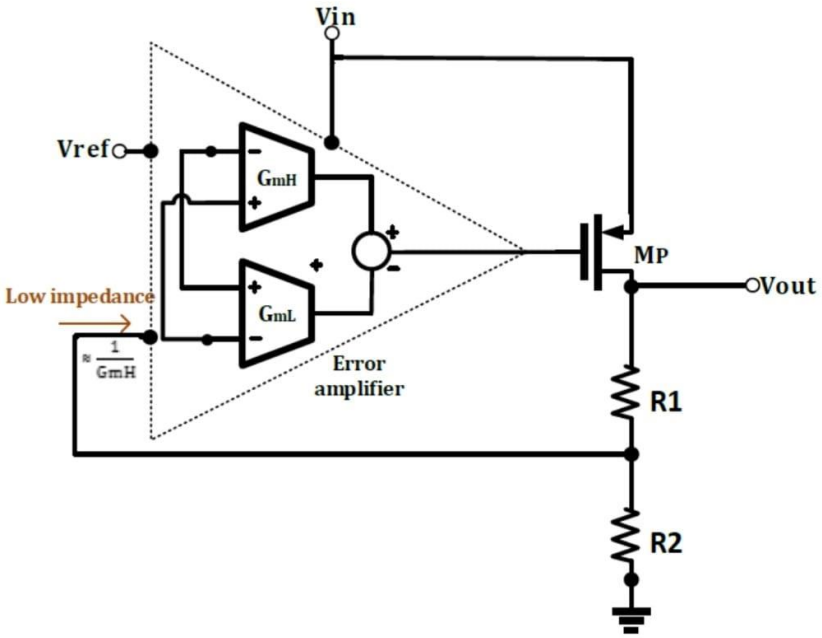


Figure.2.11: High Slew-Rate Error Amplifier architecture [8].

2.4.4 Push Pull composite power transistor

The study in [9] utilizes a push-pull composite power transistor to improve the slew-rate limitations at the gate of the power transistor MP1. Additionally, it shifts the non-dominant poles to higher frequencies, ensuring stability.

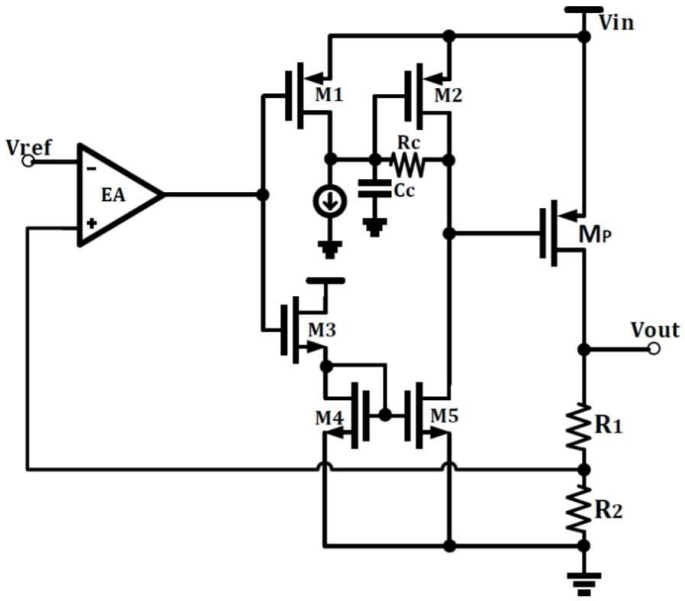


Figure.2.12: Push-Pull composite power transistor architecture [9].

. During a load current transition, this push-pull structure provides extra dynamic current at the gate of the pass device, similar to the High Slew-Rate EA topology. When a sudden increase in load current causes an undershoot at the output, so V_{out} drops quickly. This drop is detected by the error amplifier (EA), which turns off transistor M2 and turns on transistor M5. Consequently, M5 discharges the gate of the pass device MP1, enabling it to conduct the current load. Conversely, during an output overshoot transition, M2 and M5 turn on and off, respectively, allowing M2 to inject current into the gate of the pass device, reducing the current load by turning off the pass device. However, this approach consumes a high quiescent current to maintain stability.

2.5 Preliminary design of LDO

The preliminary design of a Low Dropout (LDO) regulator is a critical task in the development of efficient power management solutions. LDO regulators are essential components in modern electronic systems, providing stable and regulated output voltages with minimal voltage drop between the input and output. This characteristic makes them particularly valuable in battery-operated devices and applications where power efficiency and low noise are primary concern. In the initial design stages, several key considerations must be addressed to ensure optimal performance and reliability of the LDO regulator[1]. These include selecting the appropriate pass element (typically a MOSFET or BJT), designing a precise reference voltage, ensuring stability through proper compensation techniques, and optimizing the feedback loop. Additionally, factors such as dropout voltage, load and line regulation, transient response, and quiescent current must be carefully balanced to meet the specific requirements of the application. The preliminary design process also involves making decisions about the output capacitor, which plays a significant role in stability and transient performance. By thoroughly addressing these considerations, designers can create LDO regulators that deliver reliable performance, low noise, and high efficiency, laying a strong foundation for the subsequent detailed design and implementation phases.

Next Fig. 4.1 illustrates the architecture of the basic LDO. It consists of a NMOS differential pair as error amplifier, a PMOS pass device, and a resistive feedback network and a large output capacitor (in micro farad).

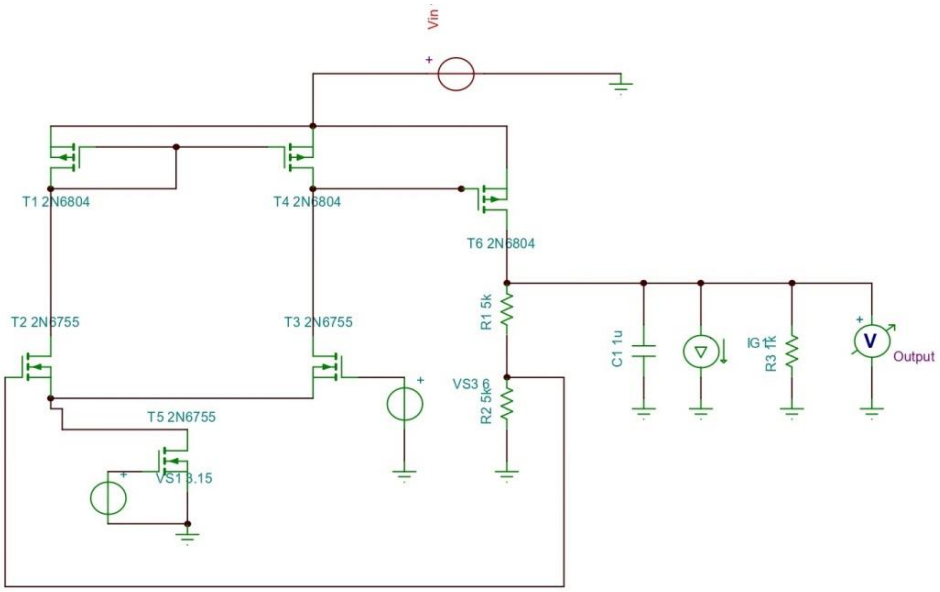


Figure2.13: Schematic view of basic LDO circuit

In this LDO circuit Type-A error amplifier consider with PMOS as a pass element due to better noise cancellation and getting high PSRR(explain in the section 2.3.3) and also use large output capacitor for better transient response because large capacitor has large discharge time and charging time[8], when large output capacitor are used then value of over shoot and undershoot become less and when smaller value of output capacitor are used then larger value of overshoot and undershoot are occurs due to smaller discharge and charging time . Large output capacitor also provide dominant pole at the output of the LDO circuit and provide stable output.

$V_{in} = 26\ v,\quad I_{out} = 8.8mA\quad ,\quad I_q = 5.14\ mA,\quad Power\ dissipation = 17.6mw\quad ,$
$Dropout\ voltage = 2v\ , PSRR = 21dB.$

$$Line\ regulation = 10\%,\ \Delta V_{out} = 5.46mv, V_{out}\ = 24v$$

$$Efficiency = 58.27\%$$

Simulation results:

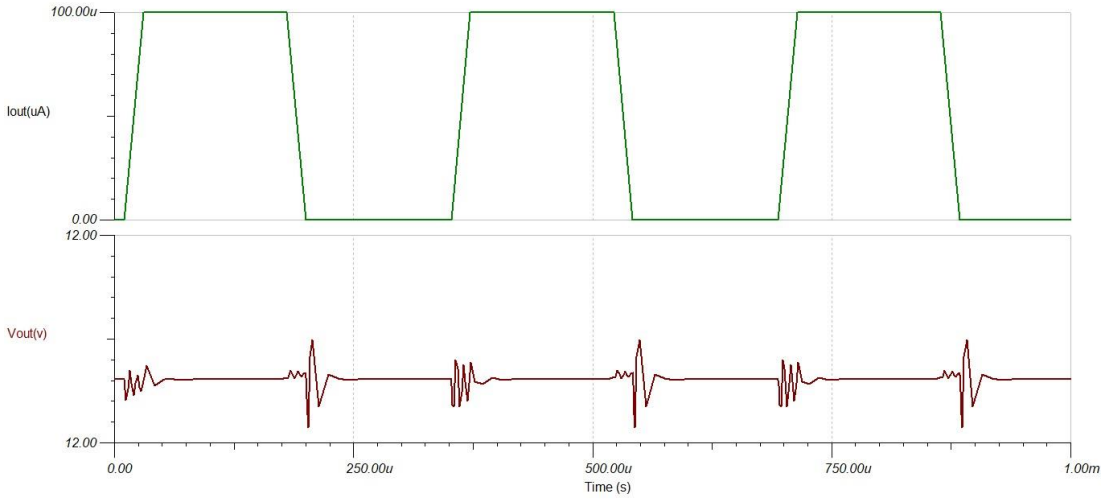


Figure2.14: Load transient response of basic LDO circuit

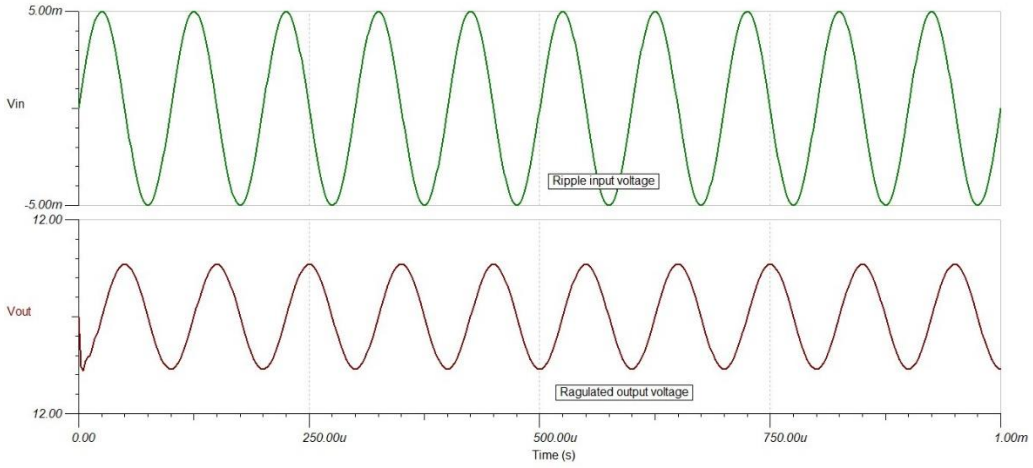


Figure2.15: Ripple rejection at no load condition

Disadvantage: Low Dropout (LDO) regulators face several challenges that can impact their performance and suitability for certain applications. These challenges arise from their inherent design principles and the evolving demands of modern electronic systems.

One major issue with conventional LDOs is their efficiency, especially at high load currents, due to the significant voltage drop across the pass element. This inefficiency results in considerable power loss ($P = (V_{in} - V_{out})I_{out}$), which generates heat that must be managed to prevent thermal runaway and ensure reliable operation. Furthermore, basic LDOs depend heavily on large external capacitors to ensure stability and manage transient response. This reliance increases the overall size and cost of the power supply solution, making it less suitable for applications where space and cost are critical factors. Ensuring stability across varying load conditions and temperatures is also challenging, as improper capacitor selection or layout can lead to oscillations and unstable output. Conventional LDOs may exhibit slower transient response compared to more advanced designs, which can be problematic in applications requiring rapid response to load changes. Additionally, basic designs may not achieve the ultra-low dropout voltages needed for modern low-voltage applications, limiting their efficiency and suitability for battery-operated devices. The characteristics of the pass element (MOSFET or BJT), directly affect the dropout voltage and achieving low dropout requires careful selection and design and that may adding to complexity. Another challenge is the relatively high quiescent current of conventional LDOs, which impacts battery life in portable applications. Minimizing quiescent current is essential for energy-efficient designs but often involves trade-offs with other performance parameters such as transient response and stability. Maintaining a constant output voltage despite changes in load current can be difficult, particularly at higher currents or with dynamic loads. Additionally, variations in the input voltage must be effectively managed to prevent fluctuations in the output voltage, requiring robust design and feedback control. In conclusion, while basic conventional LDO designs are foundational and widely used in many applications, they must address these challenges to optimize performance and meet the evolving demands of modern electronics. Through innovative design approaches and careful consideration of application-specific requirements, designers can continue to rely on LDO regulators as reliable and efficient power management solutions.

Conclusion: Basic conventional Low Dropout (LDO) regulator designs have been fundamental in ensuring reliable and efficient power management across a variety of electronic applications. These regulators are crucial for providing stable output voltages with minimal voltage drop between input and output, making them essential in low-voltage and battery-powered systems. Conventional LDO designs typically rely on external capacitors to ensure stability and improve transient response. The primary components of a basic LDO include a pass element (usually a MOSFET or BJT), an error amplifier, a reference voltage source, and a feedback loop. These components work together to maintain the desired output voltage despite variations in input voltage and load conditions.

While newer designs, such as on-chip capacitor-less LDOs, have emerged to address the challenges of space and integration, conventional LDOs remain relevant due to their proven performance, ease of design, and flexibility in various applications. Understanding the fundamental principles and components of these traditional LDO regulators provides a solid foundation for exploring more advanced and specialized power management solutions. In summary, basic conventional LDO designs continue to play a vital role in the landscape of power regulation, offering reliable performance and stability. They serve as a critical building block for more complex and integrated power management strategies, ensuring that electronic devices operate efficiently and effectively across diverse applications.

Chapter 3

3.1 Design of on chip capacitor less LDO:

Traditionally, LDO designs incorporate large external capacitors to ensure stability and effective transient response. However, in applications where space and cost are critical, such as in portable and wearable devices, using large capacitors presents significant challenges. This has led to the development of capacitor-less LDO regulators, which aim to maintain stability and performance without relying on external capacitors.

Figure 3.1 illustrates the architecture of the proposed basic CL-LDO. It includes an NMOS differential pair as the error amplifier, a PMOS pass device, and a resistive feedback network. The regulator achieves stability through Miller compensation using a local capacitor, CM.

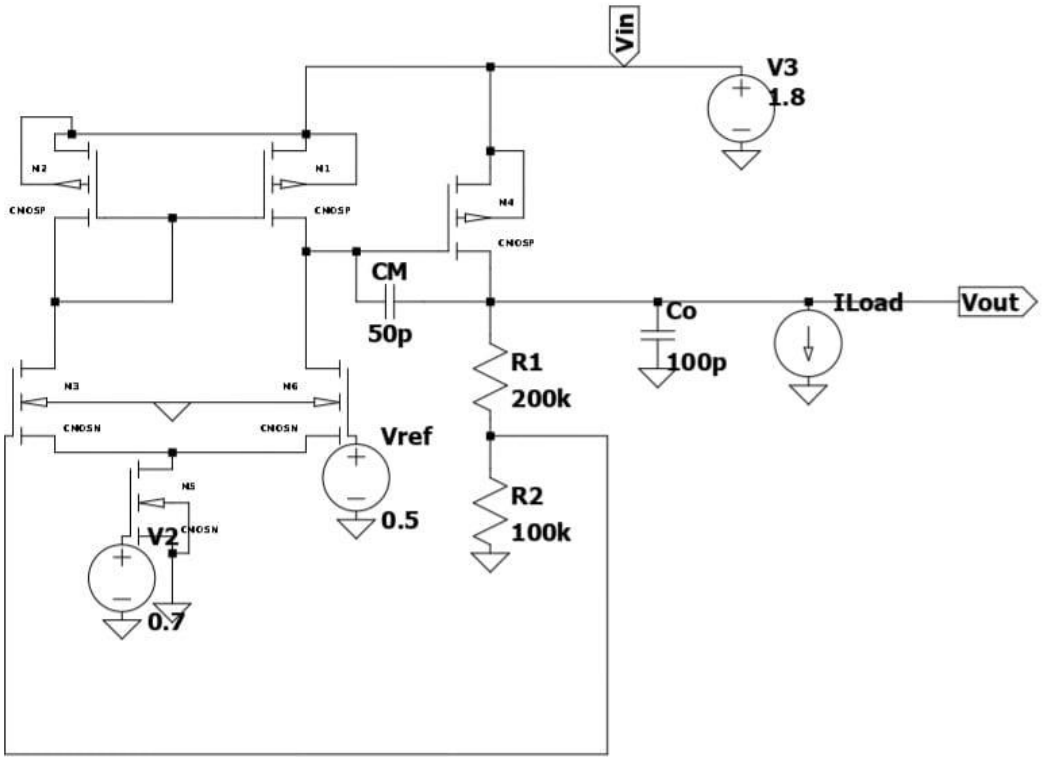


Figure 3.1: Schematic view basic capacitor less LDO

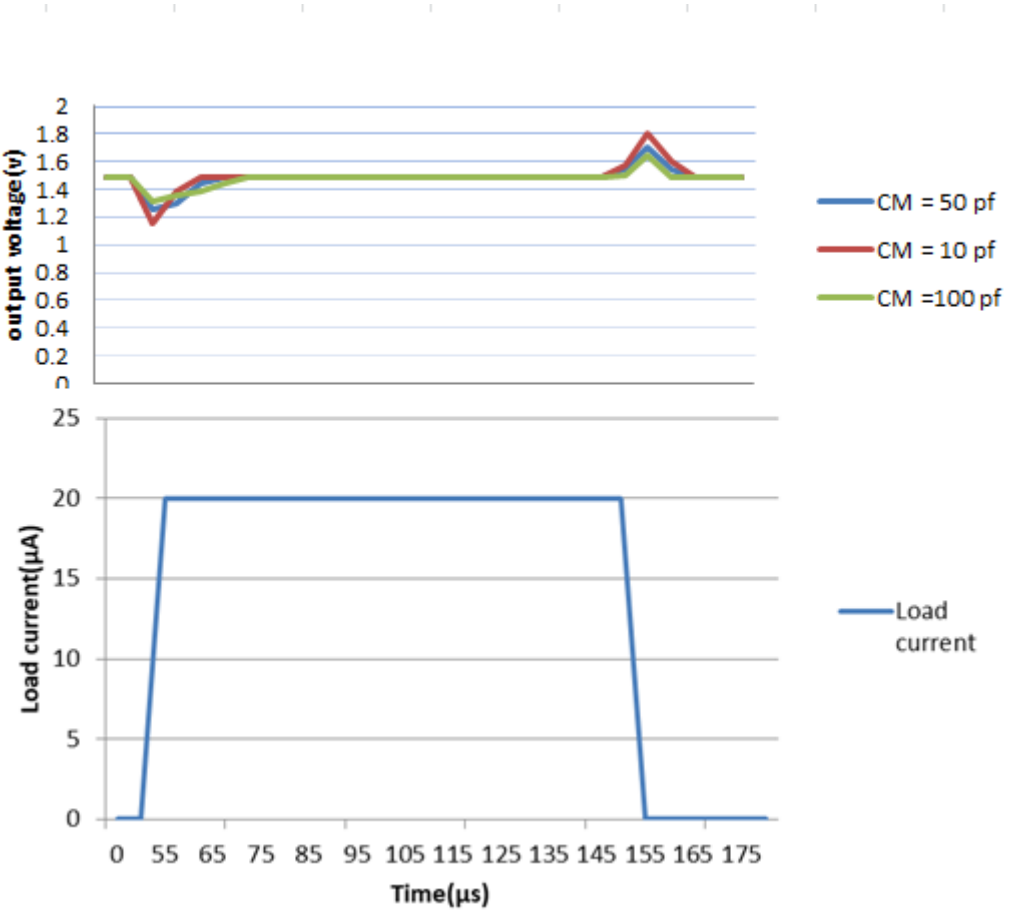


Figure3.2: Dynamic response of basic capacitor less LDO

$$I_{C_M} = C_M \frac{d(V_{pass} - V_{out})}{dt} \qquad (3.1)$$

This current is bi-directional, responding to both positive and negative changes in the output voltage. While the capacitor C_M adds a fast path between the output and the gate of the pass device, it also increases the equivalent capacitance (C_{Pass}) due to the Miller effect. Consequently, the inclusion of C_M, results in higher slew-rate current but also higher parasitic capacitance (C_{pass}). Additionally, larger values of C_M can reduce the gain-bandwidth, as it is inversely proportional to C_M.

$V_{in} = 1.8\,v$, $I_{out} = 15\ \mu A$, $I_q = 3.51\ \mu A$, $Power\ dissipation = 4.5\ \mu w$, $Dropout\ voltage = 0.3v$, $PSRR = 72\ dB$. $Line\ regulation = 10\%$, $V_{out} = 1.5$ $Efficiency = 89\%$

Compensation capacitor(pf)	$I_{C_{M_{Max}}}(\mu A)$	Undershoot value(V)	Settling time(μs)
10	0.73	0.38	40
50	0.84	0.31	60
100	0.95	0.26	110

Table3.1: undershoot transition of capacitor less LDO

$$GBW = \frac{\beta g m_1}{C_M} \qquad (3.2)$$

However, in such cases, the increased C_{pass} capacitance due to the Miller effect and the decreased bandwidth will still degrade the error amplifier's time response.

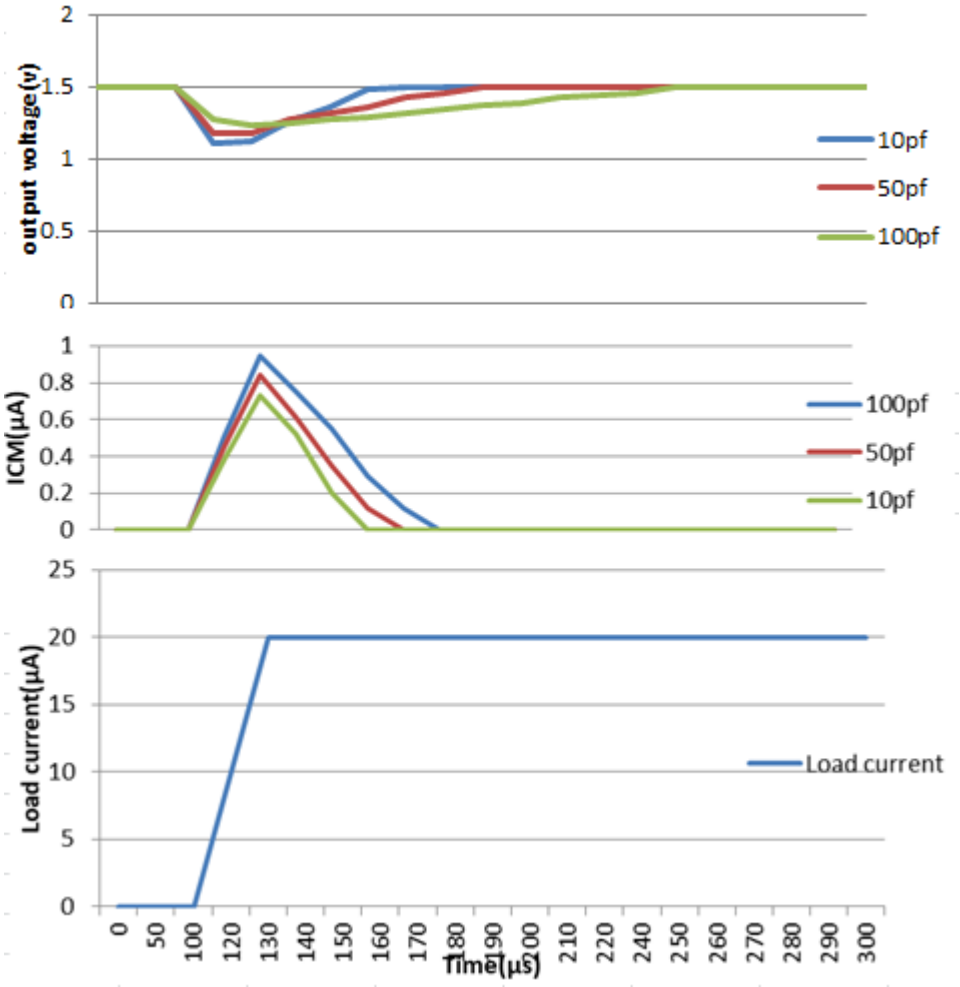


Figure 3.3: Undershoot transition of capacitor less LDO

Figure 3.2 illustrates the load transient response for different values of C_M. It is evident that the large output voltage spikes are unacceptable, with the output voltage approaching zero volts and VDD regardless of the C_M value. Figure 3.3 provides a zoomed-in view of the undershoot transition, showing the current through C_M (I_{C_M}), the EA slew-rate current (drain of M_6), and the load current transition. The increases of C_M not only affects the magnitude of the undershoot but also prolongs the settling time.

The reduction in magnitude is due to the higher current spike (I_{C_M}) injected at the gate of the pass device that discharges the equivalent capacitance C_{pass} until the output voltage stops lowering, at this moment, the injected current will rapidly decrease down to zero (Eq. 3.1). On the other hand, the larger the gate capacitance (C_{pass}) proportional to C_M because of Miller effect) the larger the propagation delay will be (settling-time).The settling-time of the overshoot transition is barely affected by the variation in capacitorC_M. The settling-time will depend on the sinking capabilities the regulator has in order to discharge and slew the output capacitor. As expected, the output capacitor discharges faster when the regulator has more sinking capabilities.

3.2 Disadvantage

Miller compensation based capacitor has some disadvantages as follows:

Miller compensation significantly increases the equivalent parasitic capacitance (C_{pass}) at the gate of the pass transistor due to the Miller effect. This increased capacitance can slow down the transient response of the LDO, particularly in fast-changing load conditions.

The addition of a Miller compensation capacitor reduces the gain-bandwidth product of the LDO. Since the bandwidth is inversely proportional to the compensation capacitance, a larger Miller capacitor can lead to a slower response, making the LDO less effective in applications requiring quick adjustments to output voltage changes.

Due to the increased capacitance and reduced bandwidth, Miller-compensated LDOs often exhibit slower transient responses. This can lead to larger voltage deviations (undershoot or overshoot) when the load current changes suddenly, which may not be acceptable in some applications.

3.3 Source of error in LDO:

Every analog circuit faces some or the other error while designing for real-world practical application. These errors prop up while doing the analog layout. Even though the circuits are designed and laid out still, they may have shortcomings. These errors may be minimized by designing the circuit carefully, but they can never be nullified. Some of the errors are discussed in the forthcoming sections.

3.2.1 Error in reference voltage:

While designing the LDO circuit, we used a reference voltage signal to compare it with our output signal and generate the negative feedback error signal. This reference signal is obtained from band-gap reference (BGR) circuits. BGR circuits provide constant voltage even in varying temperatures. However, this circuit also is not ideal. It has some error due to temperature variation, which is called curvature error.

Due to this error, output voltage gets affected directly as shown in Equation 3.3

$$\boldsymbol{V_{out} = V_{ref}(1 + \frac{R_1}{R_2})} \quad (3.3)$$

So a good analog designer must design a good BGR before designing an LDO.

3.2.2 Loop Gain

The open-loop gain of an op-amp is not infinite, as it is not ideal. So, the inverting terminal's voltage is not exactly equal to the non-inverting terminal's voltage. Therefore, proper V_{ref} at both the terminals of the error amplifier is not obtained, causing the error.

3.3.3 Mismatch in feedback resistor

In an LDO, a feedback network is always used, which causes another source of error due to the mismatch of the feedback resistor. For e.g., when R1 gets changed to $R_1 \pm \Delta R$ (shown in Figure 3.4), then V_{out} also gets changed in equation 3.4.

$$\boldsymbol{V_{out} = (1 + \frac{R_1 \pm \Delta R}{R_2})V_{ref}} \qquad \textbf{(3.4)}$$

To cancel this error, it is taken care that the resistor ratio remains constants if it is not achieved, then resistor is adjusted.

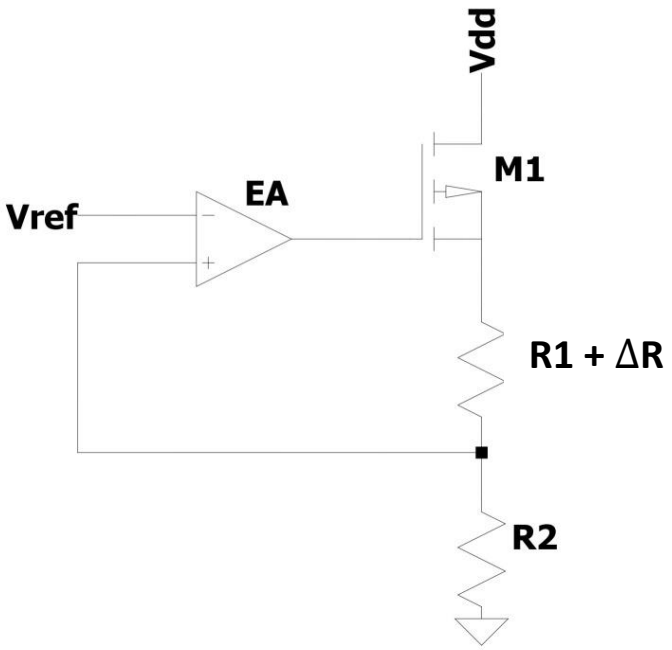


Figure3.4: Mismatch in Feedback resistor

Chapter 4

4.1 Conclusion

In this thesis work we learn about the conventional LDOs and basic capacitor less LDO their components. A regulator has to be able to regulate the output voltage under fast variations in the load current as well as in input supply with extremely low power consumption. Then we studied some critical parameters of LDO in detail for better understanding. We also discussed abut conventional LDO (capacitor based LDO) and basic capacitor less LDO. We also design and simulate conventional LDO using Tina-Ti software and design and simulate basic capacitor less LDO using 180 nm cmos technology by Ltspice simulator. Conventional LDO designs typically rely on external capacitors to ensure stability and improve transient response and it consume more power and take large area. Due to reduce the power consumption and reduce the chip area capacitor less LDO will be introduced.

In this thesis work we design a capacitor less LDO circuit using miller compensation technique. By integrating Miller compensation, these LDOs achieve stability without relying on large external capacitors, making them well-suited for compact and portable devices. However, this approach introduces certain challenges, such as increased equivalent gate capacitance due to the Miller effect, which can negatively impact the transient response and overall bandwidth of the regulator. While Miller compensation effectively stabilizes the LDO, careful design considerations are necessary to balance the trade-offs between stability, transient performance, and power efficiency. During the whole work we came across many errors of LDO and learned how to maintain.

4.2 Future work

However, there are many limitations presents in capacitor less LDO using miller compensation technique have not been improved. The main relevant are mention in the following.

1. Future work could explore advanced compensation techniques that build on the principles of Miller compensation but with improvements in stability and transient response.
2. One of the challenges associated with Miller compensation is the increase in parasitic capacitance, which can negatively impact the speed and stability of the LDO. Future research could focus on innovative circuit topologies or materials that reduce parasitic effects, thereby enhancing the regulator's overall performance without sacrificing stability.
3. While capacitor-less designs inherently reduce the need for external components, optimizing the power consumption of the LDO itself remains a priority. Future efforts could focus on reducing quiescent current and improving the power efficiency of Miller compensated designs, making them more suitable for battery-operated and energy sensitive applications.

   Miller compensation-based capacitor-less LDO regulators represent a significant advancement in power management circuits. However, there is still considerable potential for innovation and improvement. By addressing the challenges and opportunities outlined above, future research can further refine these designs, leading to more efficient, compact, and versatile LDO solutions for next-generation electronic devices.

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